PCBDesign
User Guide

For QDOS and SMSQ Operating Systems
Version 7.25
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Formally known as PCB CAD

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CONTENTS

INTRODUCTION

This section contains an introduction to PCBDesign and its facilities.

Overview of the System

PCBDesign is a package specifically designed for creating accurate printed circuit boards (PCB's) and exporting industry standard files for final fabrication and board assembly.

A project is created and edited by manipulating the various elements on the drawing board and then if necessary group these elements together to create complex components. In basic separate layer mode any one of 16 overlapping layers can be worked on at a time. The program allows for 6 copper and 16 mask layers, 2 of which are hidden. Each layer can be assigned a colour (only 7 with QDOS) for individual identification. Component reference offsets can be set to allow for production panelization.

A completed or unfinished project can be stored on a hard drive, floppy disk, memory stick, or other media for later processing. A very large library provides a source of commonly required components such as through-hole, SMD, or schematic.

PCBDesign exports multi-standard files either for media storage or serial output. PCBDesign has an absolute resolution of 1 mil (0.001 inch) over a full 16 x 16 inch drawing table.

Configuration

Minimum hardware requirements to run the program are:

QPC2 emulator (recommended system),
QL computer with at least 768K memory expansion (Trump Card), or
QXL 68040 PC adapter.

Supported device for hard copy output are:

Laser printer (Postscript).

INSTALLATION

If the program files have been unzipped on a QDOS or SMSQ system then the files may have an underscore '_' file extension character. All files in this package require dot '.' extensions. Please edit file names as required. Note the main program is written in SBasic. Should the program stop responding or behave incorrectly it may be possible to exit by pressing Ctrl Space. Typing 'cad' should resume normal operation. DO NOT use the 'RUN' command.

Floppy Disk Users

Copy the files to 2 floppy disks. Note main system files to disk 1 can be copied using 'Install.bas'

Disk 1 (Main system files)

Boot.bas	Cad.bas			
Tk.bin	Cadtk.bin	Keyword.bin		
ALogSch1.lib	Connect1.lib	Discrete.lib	Heatsink.lib	
MO-DIP1.lib	MS-DIP1.lib	MO-SMD1.lib	MO-SMD2.lib	MS-PGA1.lib
MS-SMD1.lib	MS-SMD2.lib	MS-SMD3.lib	MS-SMD4.lib	MS-SMD5.lib
SMD1.lib	Opto1.lib	TTL-Sch1.lib	TTL-Sch2.lib	
UserGuide.txt	Revisions.txt	Example.art	Diagram.art	

Disk 2 (Ball Grid Array library files)
MS-BGA(1 to 17).lib

Hard Disk Users

It is recommended that a directory called 'PCBD' is created and all files copied to it. Subdirectories can then be created to hold the project files. QPC2 users will find the program runs quite happily from the PC hard disk by using the DOS device. You can also use the DOS device to load and save artwork.

Changes to the Boot File

The 'Boot.bas' file as supplied is set up to boot from FLP1_. Note that if 'Install.bas' was used to copy files then the boot device will be the install destination device. If necessary edit line 100 to alter the boot device.
If you rename 'Boot.bas' to 'Boot' please edit line 140 and change 'Boot.bas' to 'Boot'.

SMSQ

SMSQ users can execute PCBDesign as an SBasic daughter job. Simply type:
'EX Boot.bas'.

PREPARING A DRAWING

This section contains an introduction to the basic editing facilities of PCBDesign and is aimed at the first time user. A concise description of all PCBDesign screen editor commands can be found in the section 'EDIT MODES'.

Getting Started

It would be difficult to describe the operation of the screen editor, as there is no substitute for real practice. The best way to get used to the operation of PCBDesign is to sit down in front of the screen and try out the commands. Use 'F1' as a quick reference to the majority of PCBDesign commands. If running on a machine without hi-colour support then the screen mode can be toggled using 'F10' or 'Shift F5' between modes 4 and 8. There are also three fast graphics modes with reduced information for slow machines. Use 'Ctrl F1' to select preferred mode.

Insert media containing the PCBDesign program files into your computer then run the boot program. For example if you have the program on a floppy disk then type: 'LRUN FLP1_Boot.bas'. Note SMSQ users can execute PCBDesign as an SBasic daughter job by simply typing: 'EX Boot.bas'. You will then be given the option to modify the memory allocation used for the project file. In most cases this will not be necessary and pressing the 'Enter' key will start the main program.

To exit the program press the 'Esc' key twice, then press the 'Y' key to accept. ALLWAYS exit the program in this manner. Failure to do so will not release allocated memory and may well leave the system in an unstable state. When running on QPC2, pressing the 'Esc' key three times selects a further option to minimize the QPC window.

The program has six edit modes each with its own help file. Pressing 'F1' at any time prints the appropriate file to the screen.

The Six Edit Modes:

1. Normal - New elements can be created or picked up and modified.

2. Element Edit and Formatting - An element has been picked up and can be moved or modified.

3. Label Edit - On screen editing of component Reference ID, Type/Value, Modifier, Footprint, Supplier, Supplier Stock Number.

4. Area Formatting - Area mode has been activated and can now be repositioned to encompass all elements and components that require modification.

5. Area Move and Copy - All elements and components within area can be moved or copied relative to cursor and area coordinates.

6. Text - All keys generate text. Delete is functional.

Keys that Function in all Modes (excluding text and label).

↑ ↓ ← →	Cursor keys move cross or area marker.
F1	Calls up help file.
Space Bar	Redraws and moves the screen window to centre the cursor.
1 to 9	Preset scale keys giving scales 4, 2, 1, -2, -4, -8, -16, -32, and -64. Keys '+' and '–' change scale by one step with a single click or two with a double click.
G	Grid step is incremented by 'G' key and decremented by 'Ctrl G'. Preset values are 1, 5, 10, 20, 25, 50, 100, 200, and 1000 mils. Note on PC style keyboards 'Page Up' and 'Page Dn' keys also change grid step.

Element Types

There are 4 supported element types. They are Tracks, Pads, Blocks (area of solid copper) and Text (treated as tracks by export program).

Tracks

Pressing 'T' for Track places the default track to the screen and moving the cursor will rubber-band it across the screen. Pressing 'T' again 'nails' the track down and extends the element producing a corner. The element can be 'placed' by pressing the enter key. The element can be picked up again by placing the cursor over the element and pressing the 'F' (Find) key.

Track default size and layer can be changed in normal edit mode by pressing 'Ctrl T'. This prompts for track size in mils * 5 i.e. a track width of 1 will create a track width of 5 mils. The second prompt asks for layer, this can either be a numerical value or a string of characters. Characters to select layers are: ‘b’ bottom, ‘t’ top, ‘p’ power, ‘g’ ground, ‘s1’ signal 1, ‘s2’ signal 2, ‘tss’ top silk screen, ‘tsr’ top solder resist, ‘tsp’ top solder paste, ‘tm’ top mechanical, ‘bss’ bottom silk screen, ‘bsr’ bottom solder resist, ‘bsp’ bottom solder paste, and ‘bm’ bottom mechanical. Most boards will only have one or two layers and the recommended layers are 4 and 1 for upper and lower sides respectively or 5 for both sides. If at any time a track needs to 'Via' through the board to a different layer then press 'V' to input the new layer. This action automatically produces a via pad on the screen in the appropriate layer colour. If a new via pad size needs selecting then press 'Ctrl V'. Four via sizes are supported: 4=20 mil, 6=30 mil, 8=40 mil, and 10=50 mil (default). To change the width of the track press 'W', this will prompt for a new track size.

From Version 7.21 onwards track and pad sizes can be slightly modified to allow very high board densities with 8 mil (0.2 mm) track, 7 mil (0.18 mm) clearance or 4 mil (.1 mm) track, 4 mil (0.1 mm) clearance. To achieve this all even size tracks, pads and vias are reduced in size by 2 mil or all odd sizes are reduced by 1 mil. You can switch between modes by pressing the ‘|’ key. The selected mode will be saved within the project file.

Circles and Ellipses

A circle or ellipse drawn using the default track layer and size can be created by pressing the ‘0’ (zero) key. Circle/ellipse default width and height can be changed in normal edit mode by pressing ‘Ctrl 0’. This prompts for circle/ellipse X and Y radius in mils.

Finger Pads

Finger pads are constructed from either tracks or blocks. To build from tracks just lay out a track the correct width and length to match the manufacturers recommended land pattern for the first pin. To move to the next pin press the ‘H’ key to create a hidden link. Using the cursor keys move to the position for the next pin and press the ‘T’ key to carry on. Most standard Jedec land patterns have already been constructed and are in the libraries. To build from blocks please read page 7.

Pads

Pressing 'P' places the default pad to the screen and like tracks, pressing 'P' again creates another pad connected to the first as one element. This has the advantage that an IC or component carrier can be created, moved, deleted, rotated and sized as a whole. To change the layer of an individual pad press 'V' and select the required layer. Likewise to change pad size press 'W' and select the required pad. Pin numbering for netlisting assumes that two sequential pads having the same coordinates represent a single pin.

Pad default size and layer are changed the same way as track defaults by pressing 'Ctrl P'. There are 64 round, 64 square, 64 thermal and 1 specialised pad. Pad diameter is in mils * 5, so entering 's10' at the prompt will create a square pad with a diameter of 50 mil. Likewise 'r10' will create a round pad and ‘t10 a thermal pad of the same diameter. Entering 'm' will create a board marker.

Blocks

Pressing 'B' places an area of copper on the screen and moving the cursors will move this block around the screen. To vary the size of this block press the next segment key ‘>’. You can then rubber-band the opposite corner across the screen. As with track and pads, pressing ‘B’ again will create another block of identical size to the previous one. Pressing 'Enter' drops and fills the area(s) with the appropriate layer colour.

Block default size and layer can be changed in the normal edit mode by pressing 'Ctrl B'. This prompts for block width and height in mils. The third prompt asks for layer, as with all other layer selections this can be a numerical value between 0 and 15 or a string of characters.

Corner Marker

Pressing hash ‘#’ creates a board corner marker.

Panellizing Bridge

Pressing left square bracket ‘[’ creates a panellizing bridge. This is designed for a 2mm routing tool.

Schematic Dot

Pressing full stop ‘.’ creates a schematic dot (pad size 6).

Schematic Bus

Pressing comma ‘,’ creates a bus entry or exit marker. Use the 'Q' key to get the correct orientation.

Schematic Signal Port

Pressing single quotation mark ‘ creates a named signal port. Pressing ‘N’ enters netlist edit mode to a allow editing of the signal name. Note edit name before any rotations of signal port symbol.

Schematic +/- Port

Pressing forward slash '/' creates a +/- voltage supply port. Pressing ‘N’ enters netlist edit mode to allow editing of the voltage label.

Schematic Signal Ground

Pressing semi colon ';' creates a signal ground symbol.

Fiducial Marker

Pressing ‘at’ ‘@’ creates a fiducial marker that is sometimes required for optical alignment with automatic component placement. The fiducial markers position will be included in the component placement file. Note this file is only created when using the Automated Gerber and NC Drill export option.

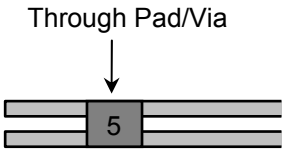
Layers

There are 6 copper and 16 mask layers, 2 of which are hidden. The layer numbers are chosen in such a way as to assign each of the 6 layers to one of the bits that make up the layer number. Typically 1 bottom, 2 ground, 4 top, 8 power, 16 signal 1, and 32 signal 2. This allows vias and pads to be assigned a layer number calculated from the layers they connect to. For example a pad connecting layer 1 and 8 would be on layer 1 + 8 = 9. In practice knowledge of how the system works is not essential. Just use the recommended layers and the design process from placing your first component through to creation of the Gerber files will be very smooth.

Physical Layer Stack
The layers are physically stacked in a particular way. The following diagrams illustrate the stack and allowable vias for various boards.

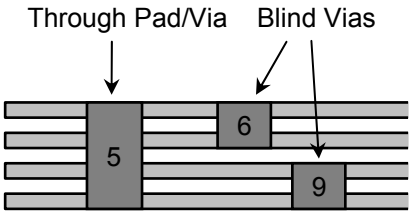
2 layer board.

Use	Layer	Stack
Top	4	1
Bottom	1	2



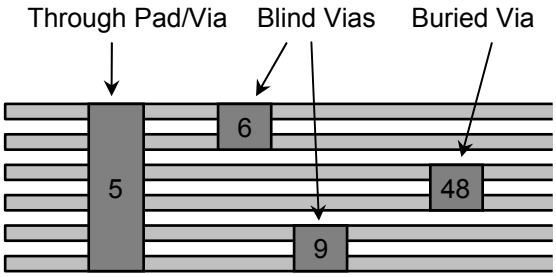
4 layer board.

Use	Layer	Stack
Top	4	1
Ground	2	2
Power	8	3
Bottom	1	4



6 layer board.

Use	Layer	Stack
Top	4	1
Ground	2	2
Signal 1	16	3
Signal 2	32	4
Power	8	5
Bottom	1	6



Vias

Vias can only bridge certain layers. These restrictions are due to the way multilayer PCB's are constructed from several 2 layer boards bonded together. You can via directly between:

Layers	Names	Via Type
1 and 4	Bottom and Top	Through
1 and 8	Bottom and Power	Blind
2 and 4	Ground and Top	Blind
16 and 32 *	Signal 1 and Signal 2	Buried

Although it's not possible to via directly between all layers, it can be done indirectly. This method always results in a through via and in some cases an offset blind via as well. To via to and from particular layers, consult the following table. Note for 4 layer boards you only need to reference the first 4 entries.

Layers	Names	Solution	Via Types
4 to 8	Top to Power	Via to 1 then move and via to 8	Through and Blind
8 to 4	Power to Top	Via to 1 then move and via to 4	Through and Blind
2 to 1	Ground to Bottom	Via to 4 then move and via to 1	Through and Blind
1 to 2	Bottom to Ground	Via to 4 then move and via to 2	Through and Blind
4 to 16 *	Top to Signal 1	Via to 1 then via to 16	Through
16 to 4 *	Signal 1 to Top	Via to 1 then via to 4	Through
4 to 32 *	Top to Signal 2	Via to 1 then via to 32	Through
32 to 4 *	Signal 2 to Top	Via to 1 then via to 4	Through
16 to 1 *	Signal 1 to Bottom	Via to 4 then via to 1	Through
1 to 16 *	Bottom to Signal 1	Via to 4 then via to 16	Through
32 to 1 *	Signal 2 to Bottom	Via to 4 then via to 1	Through
1 to 32 *	Bottom to Signal 2	Via to 4 then via to 32	Through
2 to 16 *	Ground to Signal 1	Via to 4 then move and via to 1 via to 16	Through and Blind
16 to 2 *	Signal 1 to Ground	Via to 1 then via to 4 move and via to 2	Through and Blind
2 to 32 *	Ground to Signal 2	Via to 4 then move and via to 1 via to 32	Through and Blind
32 to 2 *	Signal 2 to Ground	Via to 1 then via to 4 move and via to 2	Through and Blind
16 to 8 *	Signal 1 to Power	Via to 4 then via to 1 move and via to 8	Through and Blind
8 to 16 *	Power to Signal 1	Via to 1 then move and via to 4 via to 16	Through and Blind
32 to 8 *	Signal 2 to Power	Via to 4 then via to 1 move and via to 8	Through and Blind
8 to 32 *	Power to Signal 2	Via to 1 then move and via to 4 via to 32	Through and Blind

* Only required on 6 layer boards.

Power and Ground Planes

The Gerber-X export option allows for a much easier power and ground plane design process. To connect a track to a ground/power plane simply via through to layer 2 or 8. When using Gerber-X the time consuming job of covering the ground/power plane with copper is done for you. The copper flood fill only connects to Tracks or Vias with a Reference/ID of either 'pwr' or 'gnd' on layer 2 or 8. The flood fill avoids all other components with a clearance that can be set in the export menu. If you require a pad to connect to the ground/power plane with thermal relief then first place a round pad on either layer 6 (top copper to ground) or 9 (power to bottom copper). Then overlay a thermal pad of the same size on the required power or ground plane. This bridges the thermal clearance in 4 places.

In older versions the recommended layer for the top silk screen was 2. To allow for logical separation when working on 4 or 6 layer boards this has now been moved to layer 11. The system will automatically reassign the top silk screen when reading old project files created on pre revision 6.10 software. The recommended use for layers when designing 2 to 6 layer boards is as follows.

Num	Alpha	Layers
1	b	Bottom Copper
2	g	Ground Plane
4	t	Top Copper
8	p	Power Plane
16	s1	Signal 1
32	s2	Signal 2
63	h	Hidden

Num	Alpha	Masks
10	tsr	Top Solder Resist
14	bsr	Bottom Solder Resist
11	tss	Top Silk Screen
15	bss	Bottom Silk Screen
26	tsp	Top Solder Paste
30	bsp	Bottom Solder Paste
27	tm	Top Mechanical
31	bm	Bottom Mechanical
42	tp	Top Plating (Gold)
46	bp	Bottom Plating (Gold)
43	tre	Top Routing Edge
47	bre	Bottom Routing Edge

Num		Pads
5	tb	Top Copper to Bottom Copper
6	tg	Top Copper to Ground Plane
9	pb	Power Plane to Bottom Copper
48	ss	Signal 1 to Signal 2

Basic Routing

Now it's time for some basic routing rules. Routing is also known as "tracking". Routing is the process of laying down tracks to connect components on your board. An electrical connection between two or more pads is known as a "net".

Keep nets as short as possible. The longer your total track length, the greater the resistance, capacitance and inductance. All of which can be undesirable factors.

Tracks should only have angles of 45 degrees. Avoid the use of right angles, and under no circumstances use an angle greater than 90 degrees. This is important to give a professional and neat appearance to your board. Contrary to popular belief, sharp right angle corners on tracks only increase EMI or other problems by a small amount. The reasons to avoid right angles are much simpler - it just doesn't look good, and it may have some manufacturing implications.

"Snake" your tracks around the board, don't just go "point to point". Point to point tracking may look more efficient to a beginner at first, but there are a few reasons you shouldn't use it. The first is that it's ugly, always an important factor in PCB design! The second is that it is not very space efficient when you want to run more tracks on other layers.

Always take your track to the center of the pad, don't make your track and pad "just touch". There are few reasons for this. The first is that it's sloppy and unprofessional. The second is that future versions of PCB Design may not think that the track is making electrical connection to the pad. Proper use of the snap grid will avoid problems here.

Use a single track, not multiple tracks tacked together end to end. It may make no difference to the look of your final board, but it can be a pain for future editing. Often you'll have to extend a track a bit. In this case it's best to delete the old one and place a new one. It may take a few extra seconds, but it's worth it. People looking at your finished board may not know, but YOU'LL know! It's the little touches like this that set good PCB designers apart.

Only take one track between 100 thou pads unless absolutely necessary. Only on large and very dense designs should you consider two tracks between pads. Three tracks between pads is not unheard of, but we are talking seriously fine tolerances here.

For high currents, use multiple vias when going between layers. This will reduce your track impedance and improve the reliability. This is a general rule whenever you need to decrease the impedance of your track or power plane.

Don't "drag" tracks to angles other than 45 degrees

"Neck down" between pads where possible. E.g. a 10 thou track through two 60 thou pads gives a generous 15 thou clearance between track and pad.

If your power and ground tracks are deemed to be critical, then lay them down first. Also, make your power tracks as BIG as possible.

Keep power and ground tracks running in close proximity to each other if possible, don't send them in opposite directions around the board. This lowers the loop inductance of your power system, and allows for effective bypassing. With surface mounted components it should be possible to use the bottom layer mostly as a ground plane.

Keep things symmetrical. Symmetry in tracking and component placement is really nice from a professional aesthetics point of view.

Don't leave any unconnected copper fills (also called "dead copper"), ground them or take them out. If you are laying out a non-plated through double sided board, then there are some additional things to watch out for. Non-plate through holes require you to solder a link through the board on both the top and bottom layer.

Try and use through hole component legs to connect top tracks to bottom tracks. This minimizes the number of vias. Remember that each via adds two solder joints to your board. The more solder joints you have, the less reliable your board becomes. Not to mention that that it takes a lot longer to assemble.

Working to Grids

A major rule of PCB design, and the one most often missed by beginners, is to lay out your board on a fixed grid. This is called a “snap grid”, as your cursor, components and tracks will “snap” into fixed grid positions. Not just any size grid mind you, but a fairly coarse one. 100 mil is a standard placement grid for very basic through hole work, with 50 mil being a standard for general tracking work, like running tracks between through hole pads. For even finer work you may use a 25 mil snap grid or even lower. Many designers will argue over the merits of a 20 mil grid versus a 25 mil grid for instance. In practice, 25 mil is often more useful for boards using mostly through hole components as it allows you to go exactly half way between 50 mil spaced pads and 20 mil is better for high density boards populated with mostly SMD components.

Why is a coarse snap grid so important? It’s important because it will keep your components neat and symmetrical; aesthetically pleasing if you may. It’s not just for aesthetics though - it makes future editing, dragging, movement and alignment of your tracks, components and blocks of components easier as your layout grows in size and complexity.

A bad and amateurish PCB design is instantly recognizable, as many of the tracks will not line up exactly in the center of pads. Little bits of tracks will be “tacked” on to fill in gaps etc. This is the result of not using a snap grid effectively.

Good PCB layout practice would involve you starting out with a coarse grid such as 50 mil and then using a progressively finer snap grid if your design becomes “tight” on space. Drop to 25 mil and 10 mil for finer routing and placement when needed. This will do 99% of boards. Make sure the finer grid you choose is a nice even division of your standard 100 mil. This means 50, 25, 20, 10, or 5 mil. Don’t use anything else, you’ll regret it.

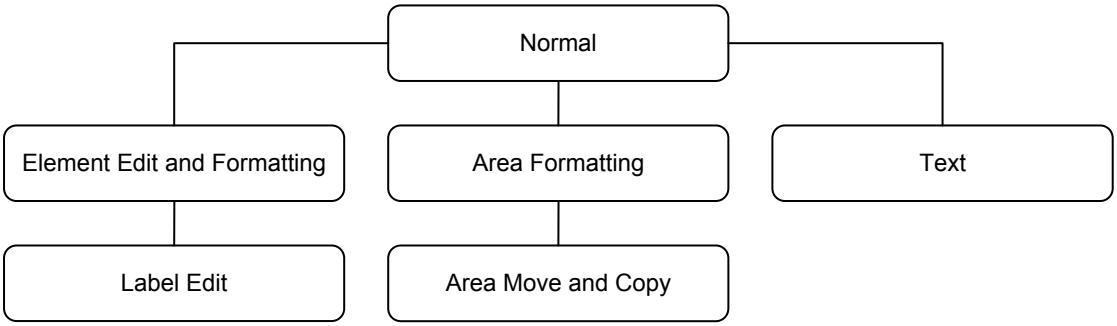
The only time you need to use the 1 mil grid is when routing tracks to metric components. But even then its best to initially route on a grid of 5 mil up to the metric device and only change down to 1 mil as close to the component as possible.

Use keys ‘G’ and ‘Ctrl G’ (Page Up, Page Down) to switch between different snap grids. There is also a “visible” grid that can be toggled on and off using the ‘F3’ key. The visible grid is displayed as a background behind your design and helps you greatly in lining up components and tracks. The colour of the visible grid can be change using ‘Ctrl F3’.

High Density Modes

There are two special modes for working at very densities that approach the limits of most PCB fabrication companies. To select these modes press the ‘|’ (pipe) key.
‘High Density’ mode optimizes track, pad and via sizes to allow a track to track spacing of 15 mil. Thus you should select a working grid of 5 mil and use track size 2 for signal traces. In high density mode all even track, pad and via sizes are reduced in size by 2 mil, therefore track size 2 has a width of 8 mil and with a track to track spacing of 15 mil the gap works out at 7 mil.
‘Ultra High Density’ mode optimizes track, pad and via sizes to allow a track to track spacing of 8 mil. Thus you should select a working grid of 1 mil and use track size 1 for signal traces. In ultra high density mode all odd track, pad and via sizes are reduced in size by 1 mil, therefore track size 1 has a width of 4 mil and with a track to track spacing of 8 mil the gap works out at 4 mil. On a BGA package with a pin to pin pitch of 0.8mm (31.5 mil) you can pass two tracks between pins.

EDIT MODES



1. Normal Mode

This mode is always returned to after executing an Element/Area format, or Text mode command. File access and default parameter changes are possible in this mode. As always, pressing ‘F1’ shows which keys are active.

Disk Functions

Ctrl I — Path:
Any valid directory device is acceptable i.e. 'FLP2_', ‘WIN1_Art1_’, etc. Note that any invalid path/device names are rejected.

Ctrl L — Load Project:
This lists all projects and directories in the current path. Use cursor keys and 'Enter' to select project or directory. To move up a directory level select ‘..’. The selected project file is loaded. Note that it is normal practice to press ‘Esc’ to start a new project before loading. However it is possible to merge two or more projects by not performing this action. One problem with merging projects is they will overlay each other. The solution is to move the cursor and perform a relocate between loads.
QL users would be wise to be in screen mode 4 before loading files. Mode 4 allows up to 143 files to be selectable.

Ctrl Shift L — Import Gerber or Bitmap Files:
On entry you will be prompted to press 'G' or 'B' to select the import file type. On selection the program lists all Gerber or Bitmap files in the current path. On loading a Gerber file you will be prompted to select the layers for tracks and pads. This feature allows import of designs from most other CAD packages that export Gerber. Please note the conversion operation may not always be successful and considerable reworking may be required. Bitmap images should be in 1,4, or 8 bits per pixel format and copper is placed on black areas of the image. Resolution is fixed at 500 dpi.

Ctrl F — File Length:
This indicates the current size of the project in memory. This information may be useful if the storage medium has limited space.

Ctrl S — Save Project File:
This prompts for a file name to save the current project to the current path. Before saving or exporting fabrication files it is good practice to move the cursor to the bottom left of the artwork and then press 'R'. This relocates the artwork to ensure correct offsets. Note that QL users should keep the number of saved files in a given directory below 143. If more files are within a directory then some will not be available to load again due to screen size restrictions.
A backup of the current work is done every 5 minutes and saved into a file called ‘Backup.art’

Ctrl D — Delete Current File:
This prompts for conformation to delete the current project or library file.

Ctrl Shift S — Save Library File:
Same operation as ‘Save Project File’, but saves with the ‘.lib’ extension.

Cursor Functions

F3 — Grid Marker:
This toggles the grid marker off and on. When active, a green grid of either 5, 50 or 500 mils dependent on scale is placed on the screen as an overlay.

Ctrl F3 — Grid Colour:
This switches on the grid marker and selects the grid colour in a ‘round robin’ fashion.

R — Relocate:
Changes the project coordinates so the present cursor position becomes 0,0.

O — Origin:
Moves the cursor to coordinate 0,0.

G — Inc Grid:
Increments the grid step ('Page Up').

Ctrl G — Dec Grid:
Decrements the grid step ('Page Down').

+ , - — Scale:
A single key click changes the scale by a factor of 2 and double by a factor of 4.

Global Element Modification

S — Size:
Prompts for element type to modify i.e. ‘T’, ‘P’ or ’L’ (Track, Pad or Label). After selecting track, pad or label you will then be prompted for the size to be globally changed.

Ctrl X — Layer EXchange:
Prompts for two layers to be exchanged.

Ctrl Shift X — Layer Change:
Prompts for layer to be changed. Note undo is available after this operation.

Element Selection

F — Find:
Picks an existing element up and moves into Element Edit and Formatting mode. An element can only be picked up if the cursor is within one grid step of a element coordinate i.e. the corner or end of an track, the centre of a pad or the corner of a block. If the wrong element is picked up subsequent Finds will select the next nearest element.

L — Library:
Allows selection of a range of predefined components from the library file on disk. The components available are listed in Appendix A. If a text string is entered a search first looks for a match on the component Footprint and then on the Type/Value.

F5 — View Library:
This toggles the screen between the current design file and one of several library files for component retrieval and library editing purposes. See page 23.

F6 or Shift F1 — Library Select:
After pressing ‘F5’ to view the libraries this loads all the library files in a ‘round robin’ fashion.

F7 or Shift F2 — Library Load:
After pressing ‘F5’ to view the libraries this allows you to directly load a particular library file.

Other Commands

X	X Mirror: Global mirror around the X axis.
Y	Y Mirror: Global mirror around the Y axis.
Q	Clockwise Rotate: Global clockwise rotate through 90 degrees.
Ctrl Q	Anticlockwise Rotate: Global anticlockwise rotate through 90 degrees.
Ctrl Shift G	Grid Set: Sets all coordinates to nearest grid step.
A	Area: Invokes 'Area Formatting Mode'.
U	Undo: Deletes any changes made after last Area edit or global rotate.
M	Mask: Assigns screen colours and descriptions to layers. Use ↑ ↓ cursor keys to select layer, ← → cursor keys to change colour, 'D' to edit the description, and 'O' to switch layers on or off. It is advisable to only change the layer descriptions when absolutely necessary and only then edit the least used. For example you could change the plating layers to guide a milling tool. Pressing the 'R' key restores the default layer descriptions. When designing complex multilayer boards it can be helpful to switch all top or bottom layers off. Pressing either 'T' or 'B' keys will do this. You can also switch off all mask layers leaving only copper layers by pressing the 'C' key. Pressing 'A' will switch on all layers and restore colours to default values.
Ctrl H	Hole Editor: This starts up a NC drill size editor. Simply navigate to the required pad and press 'Enter' to edit the associated NC drill size. Pressing 'R' or 'S' switches between round and square pads.
H	Holes: Toggles NC through-hole view on or off. Note colour is fixed to white.
F2	Export: Export program to produce Gerber, NC Drill, HP-GL, Dot matrix, or Postscript.
F9 or Shift F4	Colour Scheme: In Hi-colour mode, this selects various colour schemes.
I	Metric to Imperial Calculator: This allows you to quickly convert metric measurements in mm to imperial inches.

2. Element Edit and Formatting Mode

This mode is invoked whenever an element has been picked up or created. The element being formatted is highlighted in white. The Pad or the Track segment is highlighted in cyan. An element once picked up, may be moved about the screen as a whole or just the segment (corner). This whole/corner mode is toggled by pressing either 'E' (Edit Mode) or ‘F4’. Library components are normally unaffected by the ‘Edit Mode’. Pressing 'Ctrl E' releases the 'Edit Library Lock' and enables normal editing of library components.

Cursor Functions as normal mode.

Element Editing

K — Kill:
Removes the element or component completely.

D — Delete Segment:
Removes the segment of the element the cursor is attached to. The cursor moves to the next segment nearest the start of the element. This function will refuse to kill the element completely, leaving a minimum length element.

C — Copy:
Duplicates the element, drops the original and keeps the copy in Element editing mode.

/ — Reverse:
Reverses the order of the element. This is will be useful with future releases of PCBDesign incorporating netlists See Appendix C.

> — Next Segment:
Move the cursor toward the end of element ('End').

< — Last Segment:
Move the cursor toward the start of element ('Home').

X — X Mirror:
Mirrors element or component around the X axis.

Y — Y Mirror:
Mirrors element or component around the Y axis.

Q — Clockwise Rotate:
Rotates element or component clockwise.

Element Formatting

Ctrl Q — Anticlockwise Rotate:
Rotates element or component anticlockwise.

S — Size:
Prompts for new element size (changes the complete element).

W — Width:
Changes track or pad size for part of element.

L — Layer:
Prompts for new element layer. This removes any vias if present from the element (changes the complete element).

Ctrl X	Layer EXchange: Prompts for two layers to be exchanged.
Ctrl V	Via Size: Changes via size i.e. 4=20 mil, 6=30 mil, 8=40 mil, and 10=50 mil.
V	Via: Asks for new layer to via through to.
I	Read Library ID: This reads the components library ID.
Ctrl I	Library ID: Allows you to set or edit the component Library ID. This can be any integer from 1 to 32000. Note that the component Footprint and Type/Value labels have priority when performing a library search.
Ctrl K	Krump Component: This deconstructs components back into separate elements by removing the library ID.
N	Label Edit: Enters Label Edit Mode.
Z	NC Drill SiZe: At boot up all pads are given a calculated drill size. This allows a global change to particular pad sizes. Entry is in millimetres. Note this does not effect hole sizes for vias.

3. Label Edit Mode

Tab	Label Select: This selects the element/component label to be edited in a 'round robin' fashion. Please note the first 6 label blocks have predefined usage. 1. Reference ID Example: ‘R1’ 2. Type/Value Example: ‘220R’ 3. Modifier Example: ‘0.063W’ 4. Footprint Example: ‘0603’ 5. Supplier Example: ‘Farnell’ 6. Supplier Stock Number Example: ‘933-0801’
Shift Tab	Label Select: Same as Tab but reversed ‘round robin’.
↑ ↓ ← →	Position: Positions label by 1 grid step.
Alt ↑ ↓	Size: Adjusts the label text size. Label Track Width: Use the global size key ‘S’ in normal mode.
Alt ← →	Attributes: Changes text orientation and mirror attributes.
Ctrl L	Layer: Use to change label layer.
Ctrl O	On/Off: Toggles label visibility on/off. Note only the six predefined labels can have visibility switched off.
G	Inc Grid: Increments the grid step.('Page Up')
Ctrl G	Dec Grid: Decrements the grid step.('Page Down')

Label Edit Schematic Logic Symbols

The character set is identical to the QL apart from a few special schematic logic symbols.

Ctrl 1	Amplified Left
Ctrl 2	Amplified Right
Ctrl 3	Passive Pull Up
Ctrl 4	Passive Pull Down
Ctrl 5	Open Circuit
Ctrl 6	Open Circuit H-Type
Ctrl 7	Open Circuit L-Type
Ctrl 8	Analogue
Ctrl 9	Tri-state
Ctrl 0	Postponed
Ctrl -	Hysteresis
Ctrl =	Generator

Other logic symbols, for example Invert or Direction are drawn along with the schematic symbol.

4. Area Formatting Mode

This mode is entered by pressing 'A' in normal edit mode. The old cursor position forms one corner of a box that is rubber banded into position with the cursor keys. Pressing any of the following command keys will effect changes to all elements and components within the box area. Any changes made by, or after, an area command can be removed by the 'U' Undo function. If the box has been incorrectly placed, 'Esc' or 'Enter' exits this mode. Note text and components need to be completely within the area. However single library elements can be modified with the ‘Edit Library Lock’ switched off.

D	Delete: Removes all elements and components within area.
X	X Mirror: Mirrors all elements and components within area around the X axis.
Y	Y Mirror: Mirrors all elements and components within area around the Y axis.
Q	Clockwise Rotate: Rotates all elements and components within area clockwise.
Ctrl Q	Anticlockwise Rotate: Rotates all elements and components within area anticlockwise.
M	Move: Returns the cursor and enters Area move mode.
C	Copy: Returns the cursor and enters Area copy mode.
Ctrl X	Layer EXchange: Prompts for two layers to be exchanged.
Ctrl Shift X	Layer Change: Prompts for layer to be changed.
B	Build: Builds component for library. See page 23.
O	Reference Offset: Component reference offset. This adds a fixed numerical offset to components that is added to the Reference ID when exporting bill of materials or placement files. This allows several boards to be panellized to reduce production costs. For example two boards may have capacitors both referenced as C1 but with different values. However if one board has an offset of 100 and the other 200, the export files will reference them as C101 and C201.

5. Area Move and Copy Mode

The area within the box will be moved or copied by the relative difference between the cursor and the corner of the box that was active when 'M' was pressed. Pressing 'Enter' will execute the function or 'Esc' to terminate.

6. Text Mode

Text Mode is entered by pressing 'W' (Words) and exited by pressing 'Enter' or 'Esc'. On entering text mode a 256 character text buffer is cleared ready for input. The buffer stores file location, size and layer so that the delete key can function even when text size has been changed within text mode. The characters stored in the buffer can all be repositioned by using the cursor keys in combination with the 'Alt' key. People with a PC style keyboard may find that 'Shift ↑', 'Shift ↓', 'Home' and 'End' can be used. All text keys are active. Text size, width and layer can be changed either in text or normal mode by pressing 'Ctrl W'. The prompt first asks for text height and width. These values represent 5 mil per unit. i.e. 20 sets the text height to 100 mil. To create mirrored text, supply negative numbers. The third prompt asks for text size. This is the track width the text is drawn with, in multiples of 5 mil. And lastly layer, the recommended layer for the top silk screen mask is 11.

POINTER ENVIRONMENT

Version 7.00 introduced optional control using the pointer interface. This allows the user to control the cursor position using a mouse and to activate common commands with the mouse buttons.

Since the pointer interface for this program is still considered beta and the author still prefers cursor control, the mouse can be toggled on and off using the '*' (shift 8) key.

In normal mode the left button can pick and drop elements and components and the right button redraws the screen.

In element edit mode the left button drops the element or component and the right button extends the element by adding a pad or track for example.

In area mode the left button activates area move and the right button area copy. The mouse can then move the cursor to the required new location and the left button then completes the area move or copy. If you want to abort the operation just press the right button.

LIBRARY

The Library feature allows the most commonly used components to be recalled from a library file. A full list of supplied components can be found in Appendix A.

Recalling a Library Element

There are three methods for selecting library components.

1. Whilst in normal mode pressing 'L' invokes a prompt for a Library ID number or component description. The description will be compared with the Footprint and Type/Value labels. Note that the Footprint is given priority over the Type/Value. On pressing the enter key a search is made of all the library files for the nearest match. If found the component appears in Edit Mode.

2. Press 'F5' to select library files, then if necessary press 'F6' or 'Shift F1' to select the required library. Pick up the required component and press 'F5' again. The library component will then be taken back to your project.

3. Press 'F5' to select library files. Then press 'F7' or 'Shift F2' to select and load a library as you would a project. As with method 2, pick up the required component and press 'F5' to return it to your project.

Creating a New Library Component

The system comes supplied with a large number of library components.
If others are required then:

1. Press 'F5' to move to library files.

2. Press ‘F6’ to select an existing library or ‘ESC’ to clear memory to start a new library file.

3. Construct the new component using tracks, pads, blocks etc. Orientation is important if the component comes supplied on a reel and automatic board assembly is to be used. Construct the new component at zero degrees according to the IPC-7351 standard. There are three main standards that define component orientation and the most common one is IPC-7351. According to this standard most 2 pin devices have pin 1 to the left. Devices with more than 2 pins have pin 1 at the top left. Note if the device has numbered pins then ensure that the pads, tracks (finger pads), or blocks that represent them are in the correct order. Also note that all devices require a solder resist mask and SMD devices require a solder paste mask. Generally the solder paste mask is identical to the land pattern and the solder resist is 5 mil larger all round. Note that the placement file uses the existence of a solder paste mask to determine whether the device is surface mounted.
   Finally add the mechanical layer. This determines device position and orientation. Find the centre location of the component and draw a line from here to the top left corner of the device then carry on to the top right, bottom right, bottom left, and back to the top left. Change the line to size 0 and layer ‘tm’ top mechanical or ‘bm’ bottom mechanical.
   It would be a good idea to examine some existing library components before constructing your own.

4. Press ‘A’ and surround all the elements you require in the new component. Note any element not entirely within the defined area will not be included in the new component.

5. Press ‘B’ to build the new component within the defined area. This action builds the component and prompts you for a Library ID. This ID number can be any integer from 1 to 32000. Please reserve 7000-7999, 4000-4999 for 7400 and 4000 series logic. If the number is greater than 7499 then simply set the Library ID to 32000. The library search will still retrieve the device using the component Footprint or Type/Value.

6. Use the ‘F’ key to drop and pick up the finished component ensuring you have hold of a numbered pin or pad (the pin number will show at the bottom left of the screen).

7. Use the ‘N’ key to enter Label Edit Mode and enter Reference ID, Type/Value, Modifier, and Footprint. For example a resistor would typically have the following information:
   Reference ID ‘R?’
   Type/Value ‘?R’
   Modifier ‘?W’
   Footprint ‘0603’

8. Press ‘Ctrl I' to ensure the path is correct i.e.: 'win1_pcbd_' and change if necessary.

9. Press ‘Ctrl Shift S’ to save the new file with the ‘.lib’ extension. This action will also copy any previously existing library file with the same name to a ‘.bak’ file.

If you wish to deconstruct a component then first pick it up and then press ‘Ctrl K’ to ‘Krump’ the component.

Metric Measurements

Modern components quite often have a metric pin to pin pitch. The common pitches are: 0.4, 0.5, 0.65, 0.8, 0.95, and 1mm. These pitches can be implemented quite accurately by using a repeated sequence in mils.

The sequences are:

0.4 mm	16, 16, 16, 15 mils
0.5 mm	20, 20, 19 mils
0.65 mm	26, 25 mils
0.8 mm	32, 31 mils
0.95 mm	38, 37 mils
1 mm	40, 39 mils

PRODUCING EXPORT FILES

Main Export Menu

Pressing ‘F2’ in normal edit mode invokes the ‘Main Export Menu’. To change the plot parameters simply press the appropriate key. The plot parameters are dynamic and vary depending on the selected export format. When the parameters are correct, press 'Esc' or 'Enter' to move to the ‘Element and Layer Select Menu’.

Main Menu

E — Export Format:
This Toggles the export format between;
1. Gerber.
2. NC Drill.
3. PDF.
4. Postscript.
5. Bill of Materials.

P — Path:
Any valid serial, parallel, or directory device is acceptable i.e. 'FLP2_', ‘WIN1_Gerber_’, ‘SER1’ ,or ‘PAR1’ etc. Note that any invalid path/device names are rejected.

F — Filename:
The project name is used here, but you can edit and change it.

X — X Offset:
This offsets the plot along the X axis in mils.

Y — Y Offset:
This offsets the plot along the Y axis in mils.

M — Scale Multiplier:
Plots are scaled up by the number assigned to ‘M’. For example if M=2 the plot will be increased in size by a factor of 2 (double size). Note this only applies to Postscript export.

N — Scale Divider:
Plots are scaled down by the number assigned to ‘N’. For example if N=2 the plot will be reduced in size by a factor of 2 (half size). Note this only applies to Postscript export.

Export Formats

PCBDesign supports several export formats. Export formats are: Gerber, NC Drill, PDF, Postscript and Bill of Materials (BOM).

Gerber

Industry standard Gerber files can be created. All PCB fabricators will require this format. Note that from version 7.22 only 'RS-274X' format is supported.

'RS-274X' refers to an extended version of Gerber-D called Gerber-X. The apertures in Gerber-X are not limited to particular shapes and sizes. They are computed and embedded in the Gerber file making the whole Gerber export process much easier.

'RS-274X' also supports flood fill for power and ground planes. This feature uses the %IPNEG*% parameter. Some PCB fabricators may have software that cannot process this very useful parameter. Please check before sending off your Gerber files. If your fabricator supports this Gerber-X parameter then manual power and ground planes filling using blocks and tracks will be unnecessary. The flood fill will flow around tracks, pads, and text. Exceptions are elements labelled either 'pwr' or 'gnd' on the power or ground planes. Use the 'C' key to alter the flood fill clearance parameter. Clearance would typically be 10 mil. There is also the option of switching the flood fill off.

The 'Solder Resist on Layer 5' option can be used when exporting Gerber from an old PCB design that lacks a solder resist layer. This option places solder resist pads on top and below layer 5 pads.
Use the 'M' key to toggle the Modal coordinates option. Most PCB fabricators can cope with modal coordinates. The advantage is smaller Gerber files. Leading zero suppression will also reduce file size and should not be problem.

NC Drill

This produces an industry standard NC Drill file to complement the Gerber files.
Pressing the 'D' key will toggle the embedded drill size option on or off. NC drill files have been enhanced in recent years and can include all drill size information and therefore do not require a separate drill size information file.
Although strictly speaking the separate drill information file is not required with the embedded option switched on, it can be helpful since it lists the drills in metric as apposed to the embedded imperial measurements. For this reason it is always created.

Pressing the '1' key toggles the 'Drill Layer 1 Pads' option when using the 'Automatic Gerber' system. Old single sided designs may have pads on layer 1. If this is the case then either change all pads to layer 5 or toggle on the 'Drill Layer 1 Pads' option.

Assuming you have used the recommended layers in your design (See 'PREPARING A DRAWING') then a typical selection for a 6 layer board would be:

File Name	Connected Layers	Selected Layers	Selected Elements
xx5	Top Copper to Bottom Copper	5	P,V
xx6	Top Copper to Ground Plane	6	P,V
xx9	Power Plane to Bottom Copper	9	P,V
xx48	Signal 1 to Signal 2	48	P,V

Automated Gerber and NC Drill

If you have used the recommended layers in your design (See 'PREPARING A DRAWING') then you can use the new 'Automatic Gerber/NC Drill' feature by pressing the 'A' key. This simplifies the process of selecting particular layers and elements to create the Gerber, NC drill and report files. NC Drill export may not work correctly on single side boards where the pads are on layer 1. Either change all pads on single sided boards to layer 5 or use the 'Drill Layer 1 Pads' option (see NC Drill).

It is standard practice to number components on different boards used in a single project with a numbering offset. Typically 0, 100, 200, and so on. However new boards can be so densely packed that it becomes difficult to find space for three or more digit numbers on the silk screen. The solution is to number the components on each board starting from 1. The individual board numbering offset can be set in the design phase using the Area Reference Offset. See page 21. This offset will be saved in the project file.

Automated Gerber/NC Drill produces all the files required by a PCB fabrication company. Extra files created include component placement 'filenameTP.txt' and/or 'filenameBP.txt' and a 'Readme.txt' which describes important format and file information.

PDF

The PDF export is provided simply as a visual aid to get a photo realistic look of what the final board will look like. To get the best effect you will need to cover the entire board area by using a block or blocks on layer 0. Since most PCB's are rectangular a single block is usually sufficient. Note that layer 0 is not visible. If at any time you need to check the coverage then press the 'F8' key. This toggles layer 0 visibility on.

Note that due to complexities of the PDF file format, the creation time can be long. Also the files can be large due to compression not being implemented.

Note that to show the image at its best with Adobe Acrobat Reader you must untick 'Enhance Thin Lines' in 'Preferences / Page Display'.

Postscript

Postscript export allows you to directly print to most laser printers. The printing quality on most laser printers is good enough for DIY medium density boards. Although some fabrication companies do accept postscript files it makes little sense to use them. Since this is a likely export option for home / garage PCB production an option is included to print pads with holes to help guide the drill bit. Press 'H' to toggle this option on or off.

Bill of Materials

This creates a text file listing all components. Information includes Reference ID, Type/Value, Modifier, Package, Supplier, and Stock Number. The list is sorted by Reference ID. Note that to allow cross referencing to the placement files only components with mechanical outlines and correct labelling will be listed.

Element and Layer Select Menu

The second menu allows selection of element type and layer to be incorporated in the export file. The element types and layers may be toggled on or off by pressing the keys shown on the screen. Pressing 'Enter' will initiate export file creation, and pressing 'Esc' will abort the operation at any time.

Assuming you have used the recommended layers in your design (See 'PREPARING A DRAWING') then a typical selection for a 6 layer board would be:

File Name	Selected Layer	Description	Selected Elements
xx1	1	Bottom Copper	T,P,V,G
xx2	2	Ground Plane	T,P,V,G
xx4	4	Top Copper	T,P,V,G
xx8	8	Power Plane	T,P,V,G
xx16	16	Signal 1	T,P,V,G
xx32	32	Signal 2	T,P,V,G
xx10	10	Top Solder Resist	T,P, G
xx11	11	Top Silk Screen	T, G,L
xx26	26	Top Solder Paste	T, G
xx27	27	Top Mechanical	T, L
xx42	42	Top Plating (Gold)	T,P, G
xx43	43	Top Routing Edge	T
xx14	14	Bottom Solder Resist	T,P, G
xx15	15	Bottom Silk Screen	T, G,L
xx30	30	Bottom Solder Paste	T, G
xx31	31	Bottom Mechanical	T, L
xx46	46	Bottom Plating (Gold)	T,P, G
xx47	47	Bottom Routing Edge	T

NETLISTING

Although netlisting is not yet implemented, the file structure has been designed to support it. See Appendix B. If you wish to make use of the netlisting facilities available in proposed Version 8.nn then a few things must be taken into consideration.

All netlisted connections must be completed with one length of track with each end at precisely at the same coordinates as the pins to which they connect. This may frequently require two tracks on the same layer overlaid on each other heading for the same pin.

Component identification uses the Reference ID label. To set or alter the component Reference ID, first pick the component up using the 'F' key and then press 'N' to enter Label Edit Mode.

Pin Numbering Conventions

Whenever you pick up and edit an element the pin number will be displayed at the bottom left of the screen.

There are five different numbering systems in the present system:

Pads:

1. The first pad is pin 1 and the second pad is pin 2 and so on. If the coordinates for sequential pads are the same then they are both deemed to be the same pin. This allows for the placement of pads with different diameters on different layers whilst maintaining the correct pin numbering. For example a smaller pad on layer 5 followed by a larger pad on either layer 1 or 4. Note just placing the smaller pad on layer 1 and the larger on layer 4 would not produce an entry in the NC Drill file.
2. The system automatically looks for pads in an array layout and numbers them in the Jedec standard for BGA and PGA. If you have designed a new component that is incorrectly numbered as an array, then simply adding a hidden pad (layer 63 ’h’) as the last pin will force sequential numbering.
3. If the pad size is 1 (5 mil) then the pad is considered a schematic pin. A sequence of pins at the same coordinates will all assume the pin number of the last in the sequence. This allows you to cope with missing or unused pins.

Tracks:

4. The system automatically looks for tracks being used as finger pads i.e. they alternate between hidden and visible. In this situation the first visible track is numbered pin 1 and so on.

Blocks:

5. The first block is pin 1 and the second block is pin 2 and so on.

SCHEMATIC CAPTURE

Although generation of netlist files (Edith format) from schematic drawing is not yet implemented, the file structure has been designed to support it. See Appendix B. If you wish to make use of the schematic capture facilities available in proposed Version 8.nn then a few things must be taken into consideration.

To Create a Schematic Library Component

1. Press 'F5' to move to library files.

2. Press ‘F6’ to select an existing schematic library or ‘ESC’ to clear memory to start a new library file.

3. Draw the new element (preferably with track width 1 and layer 7) and press ‘Enter’ to exit ‘Element Edit and Formatting Mode’.

4. Move the cursor to pin 1 and press ‘Ctrl P’ to place a pad (preferably round size 1 and layer 7).

5. Then move to the location of pin 2 and press ‘P’ to place the next pad. Continue until the last pin and then press 'Enter'. Note that if a pin is unused or not required then place it in the same location as the previous pin.

6. Now proceed to step 4 in Creating a New Library Component.

Interconnection of Schematic Components

Each schematic component pin must have a labelled interconnection track joined to it (same coordinates). It is not necessary to track the whole route from one component to another, having multiple tracks with the same label on the required pins is sufficient. The actual diagram does not even have to be accurate only the labelled interconnections to the components need be.

COMPONENT PIN NUMBERING

To allow manual or automatic cross referencing between schematic and PCB netlist files and also library expansion, a standard for component numbering must be used. The table shown covers most components where confusion might arise.

Component	Pins 1	2	3	4	5
Thyristors	K	A	G		
Diodes	K	A			
Varicaps	K	A	A		
LED's	K K KgAr	A Ar AgKr	 Ag		
Triacs	MT1	MT2	G		
Polarized	V+	V-			
Variable Resistor	End	Adj	End		

HINTS and TIPS

1. If possible try to place diagonal tracks at 45 degrees. This can reduce EMC emissions but more importantly produces a neater looking board.

2. Always use the largest scale possible at any time (larger scales show more accurately distances between elements).

3. You can via pads as well! This can for example enable an IC socket to have pads on different layers, but still be a single element or allow for hidden pads for missing pins.

4. Always backup project files often (a glitch on the mains supply could ruin many hours work).

5. Although the system was not designed for it, you could use ‘F5’ to switch between two different PCB projects. To do this simply press ‘F5’ to go to the library and clear the memory using the ‘Esc’ key. Then either load an existing project or start a new one. The downside of course is the loss of the library feature.

COMPILING with TURBO

The program has been successfully compiled using ‘Turbo’. However please note some SMSQ specific extensions have been used and will cause problems on non SMSQ systems (QL). This is not a problem when using the interpreter since the program checks that these extensions are available before using them. The solution is to edit ‘Cad.bas’. First load ‘Cad.bas’ and go the end of the program. Then remove the remarks from the section of dummy functions and procedures that you will find there. Compiling should not then be a problem. Note the resulting compiled task should only be executed on a non SMSQ machine.
Dataspace requirements when using ‘Turbo’ vary dependent on screen resolution. 140K is required for a 1280x1024 window.

APPENDIX A

Library Components

'Connect1.lib' Connectors

5080 72 Pin Memory Simm

5100 9 Pin D Connector (Right Angle)
5101 15 Pin D Connector (Right Angle)
5102 25 Pin D Connector (Right Angle)
5103 37 Pin D Connector (Right Angle)
5104 50 Pin D Connector (Right Angle)
5105 15 Pin Mini D Connector (Right Angle)

5110 10 Pin IDC (Straight)	6110 10 Pin IDC (Right Angle)
5111 16 Pin IDC (Straight)	6111 16 Pin IDC (Right Angle)
5112 20 Pin IDC (Straight)	6112 20 Pin IDC (Right Angle)
5112 20 Pin IDC (Straight)	6112 20 Pin IDC (Right Angle)
5114 34 Pin IDC (Straight)	6114 34 Pin IDC (Right Angle)
5115 40 Pin IDC (Straight)	6115 40 Pin IDC (Right Angle)
5116 50 Pin IDC (Straight)	6116 50 Pin IDC (Right Angle)

5120 96 Pin ABC DIN 41612
5121 64 Pin AB DIN 41612
5122 64 Pin AC DIN 41612

5133 3 Pin 0.1" SIL Header	5134 4 Pin 0.1" SIL Header
5135 5 Pin 0.1" SIL Header	5136 6 Pin 0.1" SIL Header
5137 7 Pin 0.1" SIL Header	5138 8 Pin 0.1" SIL Header
5139 9 Pin 0.1" SIL Header	5140 10 Pin 0.1" SIL Header
5141 12 Pin 0.1" SIL Header	5142 14 Pin 0.1" SIL Header
5143 16 Pin 0.1" SIL Header	5144 18 Pin 0.1" SIL Header
5145 20 Pin 0.1" SIL Header	5146 22 Pin 0.1" SIL Header
5147 24 Pin 0.1" SIL Header	5148 26 Pin 0.1" SIL Header
5149 28 Pin 0.1" SIL Header	5150 30 Pin 0.1" SIL Header
5151 32 Pin 0.1" SIL Header	

5252 3 Pin Qikmate
5254 6 Pin Qikmate
5256 12 Pin Qikmate
5258 24 Pin Qikmate
5260 36 Pin Qikmate

5300 BNC Connector (Right Angle)
5301 DC Jack Socket
5302 Phono Socket (Single Right Angle)
5310 RJ11
5311 RJ11 Shielded
5321 RJ45 Shielded

5400 USB Mini-B (Through-hole)

5340 Button Cell Vertical 6340 Button Cell Vertical

'Connect1.lib' PLCC Carriers (50 mil unless otherwise shown)

1030 PLCC20
1034 PLCC28
1038 PLCC32

1042 PLCC44
1046 PLCC52
1050 PLCC68
1054 PLCC84

'Discrete.lib' Discrete Through-hole Components

5000 Corner Board Marker

5501 2 Pin 0.1"
5502 2 Pin 0.2"
5503 2 Pin 0.3"
5504 2 Pin 0.4" 0.25W Resistor
5505 2 Pin 0.5" 0.5W Resistor
5506 2 Pin 0.6"
5507 2 Pin 0.7" 1W Resistor
5508 2 Pin 0.8"
5509 2 Pin 0.9"
5510 2 Pin 1" 2W Resistor Outline

5560	TO3-2	5562	TO3-4	5564	TO3-8
5566	TO3-15				
5570	TO5-3	5572	TO5-6	5574	TO5-8
5576	TO5-10				
5580	TO18-3	5582	TO18-4		
5590	TO39-3	5592	TO39-4		
5600	TO46-2	5602	TO46-3	5604	TO46-4
5610	TO52-3				
5620	TO71-6				
5630	TO72-4				

5700 E-Line-3 (0.1" Pitch)
5702 E-Line-3 (0.05" Pitch)
5710 TO92-3 (0.1" Straight Pitch)
5712 TO92-3 (0.1" Pitch)
5714 TO92-3 (0.05" Pitch)
5720 TO126-3 (Horizontal)
5722 TO126-3 (Vertical)
5730 TO220-3 (Horizontal)
5732 TO220-3 (Vertical)
5750 Multiwatt15H (Horizontal)
5752 Multiwatt15V (Vertical)

5800	DO-35	5804	DO-41

‘MO-DIP1.lib’ Dual In-line Through-hole Devices

1500	MO-001AJ	1501	MO-001AK	1502	MO-001AL
1503	MO-001AM				
1504	MO-015AN	1505	MO-015AP		
1506	MO-016AA	1507	MO-016AB	1508	MO-016AC
1509	MO-016AD				
1510	MO-024AA	1511	MO-024AB		
1512	MO-026BA	1513	MO-026BB	1514	MO-026BC
1515	MO-026BD	1516	MO-026BE	1517	MO-026CA
1518	MO-028AA				
1519	MO-036AA				
1520	MO-038AA	1521	MO-038AB	1522	MO-038AC
1523	MO-039AA				
1524	MO-043AA				
1525	MO-103AA	1526	MO-103AB	1527	MO-103AC
1528	MO-103AD				

‘MS-DIP1.lib’ Dual In-line Through-hole Devices

1529	MS-001AA	1530	MS-001AB	1531	MS-001AC
1532	MS-001AD	1533	MS-001AE	1534	MS-001AF
1535	MS-001AG	1536	MS-001BA	1537	MS-001BB
1538	MS-001BC	1539	MS-001BD	1540	MS-001BE
1541	MS-001BF				
1542	MS-010AA	1543	MS-010AB	1544	MS-010AC
1545	MS-010AD				
1546	MS-020AA	1547	MS-020AB	1548	MS-020AC
1549	MS-020AD				
1550	MS-030AA	1551	MS-030AB	1552	MS-030AC
1553	MS-030AD	1554	MS-030AE	1555	MS-030AF
1556	MS-030AG				
1557	MS-031AA				

'MO-SMD1.lib' Dual In-line Surface Mounted Devices

9200	MO-118AA	9201	MO-118AB	9202	MO-118AC
9203	MO-118AD				
9204	MO-120AA	9205	MO-120AB	9206	MO-120AC
9207	MO-120AD				
9208	MO-137AA	9209	MO-137AB	9210	MO-137AC
9211	MO-137AD	9212	MO-137AE	9213	MO-137AF
9214	MO-137BA-1	9215	MO-137BB-1		
9216	MO-142AA	9217	MO-142AB	9218	MO-142AC
9219	MO-142AD	9220	MO-142BA	9221	MO-142BB
9222	MO-142BC	9223	MO-142BD	9224	MO-142CA
9225	MO-142CB	9226	MO-142CC	9227	MO-142CD
9228	MO-142DA	9229	MO-142DB	9230	MO-142DC
9231	MO-142DD	9232	MO-142EA	9233	MO-142EB
9234	MO-142EC				
9235	MO-150AA	9236	MO-150AB	9237	MO-150AC
9238	MO-150AD	9239	MO-150AE	9240	MO-150AF
9241	MO-150AG	9242	MO-150AH	9243	MO-150AJ
9244	MO-150AK				

'MO-SMD2.lib'

9245	MO-153AA-T	9246	MO-153AB-1-T	9247	MO-153AB-T
9248	MO-153AC-T	9249	MO-153AD-T	9250	MO-153AE-T
9251	MO-153BA-T	9252	MO-153BB-T	9253	MO-153BC-T
9254	MO-153BC-1-T	9255	MO-153BD-T	9256	MO-153BD-1-T
9257	MO-153BE-T	9258	MO-153BF-T	9259	MO-153CA-T
9260	MO-153CB-T	9261	MO-153CC-T	9262	MO-153CD-T
9263	MO-153DA-T	9264	MO-153DB-T	9265	MO-153DB-1-T
9266	MO-153DC-T	9267	MO-153DD-T	9268	MO-153DD-1-T
9269	MO-153DE-T	9270	MO-153EA-T	9271	MO-153EB-T
9272	MO-153EC-T	9273	MO-153EC-1-T	9274	MO-153ED-T
9275	MO-153EE-T	9276	MO-153EF-T	9277	MO-153FA-T
9278	MO-153FB-T	9279	MO-153FC-T	9280	MO-153FD-T
9281	MO-153FE-T	9282	MO-153FF-T	9283	MO-153GA-T
9284	MO-153GB-T	9285	MO-153GC-T	9286	MO-153GD-T
9287	MO-153HA-T	9288	MO-153HB-T	9289	MO-153HC-T
9290	MO-153HD-T	9291	MO-153JA-T	9292	MO-153JB-T
9293	MO-153JC-T	9294	MO-153JC-1-T	9295	MO-153JD-T
9296	MO-153JD-1-T				
9297	MO-187AA-T	9298	MO-187BA-T	9299	MO-187CA
9300	MO-187DA				
9301	MO-193AA	9302	MO-193AB	9303	MO-193BA
9304	MO-223AA	9305	MO-223AB	9306	MO-223BA

'MS-SMD1.lib'

9307	MS-012A/BA	9308	MS-012A/BB	9309	MS-012A/BC
9310	MS-013A/BA	9311	MS-013A/BB	9312	MS-013A/BC
9313	MS-013A/BD	9314	MS-013A/BE	9315	MS-013A/BF
9316	MS-018AA	9317	MS-018AB	9318	MS-018AC
9319	MS-018AD	9320	MS-018AE	9321	MS-018AF
9322	MS-018AG				
9323	MS-022AA	9324	MS-022AB	9325	MS-022AC
9326	MS-022B/BD	9327	MS-022B/BE	9328	MS-022B/BF
9329	MS-022CA-1/2	9330	MS-022CB-1/2	9331	MS-022CC-1/2
9332	MS-022DA-1/2	9333	MS-022DB-1/2	9334	MS-022DC-1/2
9335	MS-022DD-1/2	9336	MS-022EA	9337	MS-022FA
9338	MS-022GA-1/2	9339	MS-022GB-1/2	9340	MS-022GC-1/2

'MS-SMD2.lib'

9341	MS-024AA	9342	MS-024AB	9343	MS-024 SRAM
9344	MS-024AC	9345	MS-024BA	9346	MS-024BB
9347	MS-024BC	9348	MS-024BD	9349	MS-024CA
9350	MS-024CB	9351	MS-024DA	9352	MS-024EA
9353	MS-024FA	9354	MS-024FB	9355	MS-024FC
9356	MS-024GA	9357	MS-026A/BKA	9358	MS-026A/BKB
9359	MS-026A/BKC	9360	MS-026A/BAA	9361	MS-026A/BAB
9362	MS-026A/BBC	9363	MS-026A/BBD	9364	MS-026A/BBE
9365	MS-026A/BBF	9366	MS-026A/BCA	9367	MS-026A/BCB
9368	MS-026A/BCC	9369	MS-026A/BCD	9370	MS-026A/BCE
9371	MS-026A/BDA	9372	MS-026A/BDB	9373	MS-026A/BDC
9374	MS-026A/BDD	9375	MS-026A/BDF		

'MS-SMD3.lib'

9376	MS-026A/BEA	9377	MS-026A/BEB	9378	MS-026A/BEC
9379	MS-026A/BED	9380	MS-026A/BEE	9381	MS-026A/BFA
9382	MS-026A/BFB	9383	MS-026A/BFC	9384	MS-026A/BGA
9385	MS-026A/BGB	9386	MS-026A/BHA	9387	MS-026A/BHB
9388	MS-026BJA	9389	MS-026BJB	9390	MS-026BJC

‘MS-SMD4.lib’

9391	MS-029AA	9392	MS-029AB	9393	MS-029BA
9394	MS-029BB	9395	MS-029BC	9396	MS-029CA
9397	MS-029CB	9398	MS-029CC	9399	MS-029CD
9400	MS-029DA-1/2	9401	MS-029DB-1/2	9402	MS-029DC-1/2
9403	MS-029DD-1/2	9404	MS-029EA	9405	MS-029EB

'MS-SMD5.lib'

9406	MS-029FA-1/2	9407	MS-029FB-1/2	9408	MS-029GA
9409	MS-029GB	9410	MS-029HA	9411	MS-029HB
9412	MS-029JA	9413	MS-029JB	9414	MS-029KA

‘MS-PGA1.lib’ 0.1” Pitch Pin Grid Array Devices

9700	MS-017A/BA	9701	MS-017A/BB	9702	MS-017A/BC
9703	MS-017A/BD	9704	MS-017A/BE	9705	MS-017A/BF
9706	MS-017A/BG	9707	MS-017A/BH	9708	MS-017A/BJ
9709	MS-017A/BK	9710	MS-017A/BL	9711	MS-017A/BM

‘MS-BGA1.lib’ 1 mm Pitch Ball Grid Array Devices

9800	MS-034AAA-2	9801	MS-034AAA-1	9802	MS-034ABB-2
9803	MS-034ABB-1	9804	MS-034AAB-2	9805	MS-034AAB-1
9806	MS-034ABC-2	9807	MS-034ABC-1	9808	MS-034AAC-2
9809	MS-034AAC-1	9810	MS-034ABD-2	9811	MS-034ABD-1
9812	MS-034AAD-2	9813	MS-034AAD-1	9814	MS-034ABE-2
9815	MS-034ABE-1	9816	MS-034AAE-2	9817	MS-034AAE-1
9818	MS-034AAF-2	9819	MS-034AAF-1	9820	MS-034AAG-2
9821	MS-034AAG-1	9822	MS-034AAH-2	9823	MS-034AAH-1
9824	MS-034AAJ-2	9825	MS-034AAJ-1	9826	MS-034AAK-2
9827	MS-034AAK-1				

‘MS-BGA2.lib’

9828	MS-034AAL-2	9829	MS-034AAL-1	9830	MS-034AAM-2
9831	MS-034AAM-1	9832	MS-034AAN-2	9833	MS-034AAN-1
9834	MS-034AAP-2				

‘MS-BGA3.lib’

9835	MS-034AAP-1	9836	MS-034AAR-2	9837	MS-034AAR-1
9838	MS-034AAT-2	9839	MS-034AAT-1		

‘MS-BGA4.lib’

9840	MS-034AAU-2	9841	MS-034AAU-1	9842	MS-034AAV-2

‘MS-BGA5.lib’

9843	MS-034AAV-1	9844	MS-034AAW-2

‘MS-BGA6.lib’

9845	MS-034AAW-1	9846	MS-034AAY-2

‘MS-BGA7.lib’

9847	MS-034AAY-1	9848	MS-034ABA-2	9849	MS-034ABA-1

‘MS-BGA8.lib’

9850	MS-034ABF-2	9851	MS-034ABF-1

‘MS-BGA9.lib’

9852	MS-034ABG-2	9853	MS-034ABG-1

‘MS-BGA10.lib’ 1.27 mm Pitch Ball Grid Array Devices

9854	MS-034BAA-2	9855	MS-034BAA-1	9856	MS-034BBB-2
9857	MS-034BBB-1	9858	MS-034BAB-2	9859	MS-034BAB-1
9860	MS-034BBC-2	9861	MS-034BBC-1	9862	MS-034BAC-2
9863	MS-034BAC-1	9864	MS-034BBD-2	9865	MS-034BBD-1
9866	MS-034BAD-2	9867	MS-034BAD-1	9868	MS-034BBE-2
9869	MS-034BBE-1	9870	MS-034BAE-2	9871	MS-034BAE-1
9872	MS-034BAF-2	9873	MS-034BAF-1	9874	MS-034BAG-2
9875	MS-034BAG-1	9876	MS-034BAH-2	9877	MS-034BAH-1

‘MS-BGA11.lib’

9878	MS-034BAJ-2	9879	MS-034BAJ-1	9880	MS-034BAK-2
9881	MS-034BAK-1	9882	MS-034BAL-2	9883	MS-034BAL-1
9884	MS-034BAM-2	9885	MS-034BAM-1	9886	MS-034BAN-2
9887	MS-034BAN-1	9888	MS-034BAP-2	9889	MS-034BAP-1
9890	MS-034BAR-2	9891	MS-034BAR-1	9892	MS-034BAT-2
9893	MS-034BAT-1	9894	MS-034BAU-2	9895	MS-034BAU-1

‘MS-BGA12.lib’

9896	MS-034BAV-2	9897	MS-034BAV-1	9898	MS-034BAW-2
9899	MS-034BAW-1	9900	MS-034BAY-2		

‘MS-BGA13.lib’

9901	MS-034BAY-1	9902	MS-034BBA-2	9903	MS-034BBA-1
9904	MS-034BBF-2				

‘MS-BGA14.lib’

9905	MS-034BBF-1	9906	MS-034BBG-2	9907	MS-034BBG-1
9908	MS-034CAA-2	9909	MS-034CAA-1	9910	MS-034CBB-2
9911	MS-034CBB-1	9912	MS-034CAB-2	9913	MS-034CAB-1
9914	MS-034CBC-2	9915	MS-034CBC-1	9916	MS-034CAC-2
9917	MS-034CAC-1	9918	MS-034CBD-2	9919	MS-034CBD-1
9920	MS-034CAD-2	9921	MS-034CAD-1	9922	MS-034CBE-2
9923	MS-034CBE-1	9924	MS-034CAE-2	9925	MS-034CAE-1
9926	MS-034CAF-2	9927	MS-034CAF-1		

‘MS-BGA15.lib’

9928	MS-034CAG-2	9929	MS-034CAG-1	9930	MS-034CAH-2
9931	MS-034CAH-1	9932	MS-034CAJ-2	9933	MS-034CAJ-1
9934	MS-034CAK-2	9935	MS-034CAK-1	9936	MS-034CAL-2
9937	MS-034CAL-1	9938	MS-034CAM-2	9939	MS-034CAM-1
9940	MS-034CAN-2	9941	MS-034CAN-1	9942	MS-034CAP-2
9943	MS-034CAP-1	9944	MS-034CAR-2		

‘MS-BGA16.lib’

9945	MS-034CAR-1	9946	MS-034CAT-2	9947	MS-034CAT-1
9948	MS-034CAU-2	9949	MS-034CAU-1	9950	MS-034CAV-2
9951	MS-034CAV-1	9952	MS-034CAW-2	9953	MS-034CAW-1

‘MS-BGA17.lib’

9954	MS-034CAY-2	9955	MS-034CAY-1	9956	MS-034CBA-2
9957	MS-034CBA-1				

‘SMD1.lib’ Discrete Surface Mount Devices

9000	Fiducial Mark		
9004	YC158 Resistor Pack Horizontal	9005	YC158 Resistor Pack Vertical
9010	0402R Resistor Horizontal	9011	0402R Resistor Vertical
9012	0603R Resistor Horizontal	9013	0603R Resistor Vertical
9014	0805R Resistor Horizontal	9015	0805R Resistor Vertical
9018	1008R Resistor Horizontal	9019	1008R Resistor Vertical
9020	1206R Resistor Horizontal	9021	1206R Resistor Vertical
9022	1210R Resistor Horizontal	9023	1210R Resistor Vertical
9030	2010R Resistor Horizontal	9031	2010R Resistor Vertical
9038	2512R Resistor Horizontal	9039	2512R Resistor Vertical
9060	0402C Capacitor Horizontal	9061	0402C Capacitor Vertical
9062	0603C Capacitor Horizontal	9063	0603C Capacitor Vertical
9064	0805C Capacitor Horizontal	9065	0805C Capacitor Vertical
9066	1005C Capacitor Horizontal	9067	1005C Capacitor Vertical
9074	1812C Capacitor Horizontal	9075	1812C Capacitor Vertical
9076	1825C Capacitor Horizontal	9077	1825C Capacitor Vertical
9078	1913C Capacitor Horizontal	9079	1913C Capacitor Vertical
9082	2215C Polarised Capacitor Horizontal	9083	2215C Polarised Capacitor Vertical
9084	2220C Capacitor Horizontal	9085	2220C Capacitor Vertical
9088	2225C Capacitor Horizontal	9089	2225C Capacitor Vertical
9090	3020C Capacitor Horizontal	9091	3020C Capacitor Vertical
9092	TA Tantalum Capacitor Horizontal	9093	TA Tantalum Capacitor Vertical
9094	TB Tantalum Capacitor Horizontal	9095	TB Tantalum Capacitor Vertical
9096	TC Tantalum Capacitor Horizontal	9097	TC Tantalum Capacitor Vertical
9098	TD-E Tantalum Capacitor Horizontal	9099	TD-E Tantalum Capacitor Vertical
9122	VB Polarised Capacitor Horizontal	9123	VB Polarised Capacitor Vertical
9124	VC Polarised Capacitor Horizontal	9125	VC Polarised Capacitor Vertical
9126	VD Polarised Capacitor Horizontal	9127	VD Polarised Capacitor Vertical
9128	VE Polarised Capacitor Horizontal	9129	VE Polarised Capacitor Vertical
9130	VF Polarised Capacitor Horizontal	9131	VF Polarised Capacitor Vertical
9132	VG Polarised Capacitor Horizontal	9133	VG Polarised Capacitor Vertical
9140	SOT343 Horizontal	9141	SOT343 Vertical
9144	SC70-5 Horizontal	9145	SC70-5 Vertical
9146	SC70-6 Horizontal	9147	SC70-6 Vertical
9150	SOT23-3 Horizontal	9151	SOT23-3 Vertical
9154	SOT23-5 Horizontal	9155	SOT23-5 Vertical
9158	SOT143 Horizontal	9159	SOT143 Vertical
9160	SOT457 Horizontal	9161	SOT457 Vertical
9162	SOT89-3 Horizontal	9163	SOT89-3 Vertical
9164	SOT223 Horizontal	9165	SOT223 Vertical
9166	TO252 (DPAK) Horizontal	9167	TO252 (DPAK) Vertical
9168	TO252B (DPAK) Horizontal	9169	TO252B (DPAK) Vertical
9170	TO263 Horizontal	9171	TO263 Vertical
9172	SC-76 Diode Horizontal	9173	SC-76 Diode Vertical
9174	SOD323 Diode Horizontal	9175	SOD323 Diode Vertical
9176	SMB Diode Horizontal	9177	SMB Diode Vertical
9180	7x5mmXTAL Quartz Crystal Horizontal	9181	7x5mmXTAL Quartz Crystal Vertical
9184	7x5mmOSC Oscillator Module	9185	7x5mmOSC Oscillator Module
9190	CSTCC Ceramic Resonator Horizontal	9191	CSTCC Ceramic Resonator Vertical
9192	CSTCR Ceramic Resonator Horizontal	9193	CSTCR Ceramic Resonator Vertical

12000 Battery Lithium Ion 3.7V 150mAh

13000 Switch SPSP Omron B3U-3000P-B
13010 Switch SPSP C&K SD001

‘ALogSch1.lib' Analogue Schematic Components

10000-10009 Capacitors
10000 Non-polarised
10001 Polarized
10002 Variable
10003 Trimmer

10010-10019 Inductors
10010 Coil/Transformer ferrite
10011 Coil/Transformer iron

10020-10029 Resistors
10020 Resistor
10021 3 Pin variable
10022 3 Pin trimmer
10023 2 Pin variable
10024 2 Pin trimmer
10025 Thermistor
10026 LDR

10030-10039 Transistors
10030 NPN (bipolar)
10031 PNP (bipolar)
10032 Unijunction
10033 N-Channel (FET)
10034 P-Channel (FET)

10040-10049 Diodes
10040 Diode
10041 Zener
10042 Varicap
10043 Pin
10044 LED
10045 Thyristor
10046 Diac
10047 Triac

10050-10099 Discrete Semiconductors

‘ALogSch1.lib'

10100 Battery
10101 Signal Earth
10102 Signal Ground
10103 Aerial
10104 Plug
10105 Socket
10106 Speaker
10110 Lamp
10120 +/-Port
10130 Signal Port

10200-10299 Switches
10200 1P1W
10201 1P2W

10300-10399 OP AMP's

10400-10599 Linear IC's

10600-10699 Thermionic Devices

‘Opto1.lib’ Optoelectronics

11090 TA07-11 Kingbright 18mm Single Colour LED Matrix Display
11100 UG-2828GDEDF Univision 128x128 OLED Display
11101 FH19SC-30S-0.5SH(05) HRS Connector for above
11108 DD-9664FC-2A Densitron 96x64 OLED Display
11110 DD-160-128FC-1A Densitron 160x128 OLED Display
11111 XF2M-1215-1A Omron Connector for above
11120 COG-BT96040A Batron 96x40 LCD Display

'TTLSch1.lib' 74 Series Schematic Logic

7400A - 7400D
7401A - 7401D
7402A - 7402D
7403A - 7403D
7404A - 7404F
7405A - 7405F
7406A - 7406F
7407A - 7407F
7408A - 7408D
7409A - 7409D
7410A - 7410C
7411A - 7411C
7412A - 7412C
7413A 7413B
7414A - 7414F
7415A - 7415C
7418A 7418B
7419A - 7419F
7420A 7420B
7421A 7421B
7422A 7422B
7423A 7423B
7424A - 7424D
7425A 7425B
7426A - 7426D
7427A - 7427C
7428A - 7428D
7430
7431A - 7431F
7432A - 7432D
7433A - 7433D
7437A - 7437D
7438A - 7438D
7439A - 7439D
7440A 7440B
7450A 7450B
7451A 7451B
7453
7454
7455
7464
7465
7486A - 7486D
74125A - 74125D
74126A - 74126D
74128A - 74128D
74132A - 74132D
74133
74134
74135A 75135B
74136A - 74136D
74140A 74140B
74260A 74260B
74265A - 74265D
74266A - 74266D
74279A - 74279D
74386A - 74386D

'TTLSch2.lib' 74 Series Schematic Logic

7495
7496
7497
74107A 74107B
74109A 74109B
74111A 74111B
74112A 74112B
74113A 74113B
74114
74116A 74116B
74120A 74120B
74121
74122
74123A 74123B
74124A 74124B
74137
74138
74139
74143
74145
74147 , 74148
74150 Thru 74152
74153A 74153B
74154
74155A 74155B
74156A 74156B
74157 , 74158
74160 Thru 74163
74164
74165
74166
74167
74169
74170
74171
74172
74173
74174 , 74175
74176 , 74177
74178
74180
74181
74182
74183
74190 , 74191
74192 , 74193
74194
74195
74196 , 74197
74198 , 74199
74221A 74221B
74240 , 74241 , 74244
74242 , 74243
74245
74247 , 74248
74251
74253
74257 , 74258
74259
74261
74273
74276
74278
74280
74283
74285
74290 , 74293
74292 , 74294
74295
74297
74298
74299
74320 , 74321
74322

'TTLSch3.lib' 74 Series Schematic Logic

74323
74348
74352
74353
74354 Thru 74356
74365 Thru 74368
74373 , 74374
74375
74376
74377 Thru 74379
74381 , 74382
74384
74385
74390 , 74393
74395
74396
74399
74422 , 74423
74440 Thru 74444
74445
74446 , 74449
74465 Thru 74468
74490A 74490B
74540 , 74541
74590 , 74591
74592 , 74593
74594 , 74599
74595 , 74596
74597 , 74598
74600 , 74601 , 74603
74604 , 74606 , 74607
74610 Thru 74613
74620 , 74621 , 74623
74624 Thru 74629
74630 , 74631
74636 , 74637
74638 , 74639
74640 Thru 74642 , 74644 , 74645
74646 Thru 74649
74651 Thru 74653
74668 , 74669
74670
74671 , 74672
74673 , 74674
74681
74682 Thru 74689
74690 , 74691 , 74693
74696 , 74697 , 74699

APPENDIX B

Project File Format Version 1 (1.00 - 4.01)

This information is useful for user written programs which need to access PCB CAD or earlier EIX art files. Projects are stored in files with an '.art' extension. All coordinates are stored in 2's compliment integer form with the most significant byte highest in memory. The data file consists of a number of variable length records terminated in a header block starting with hex FF.

Construction of Element Data Block.

The construction of an Element Data Block consists of:

1. 5-Byte Header Block.
2. 5-Byte layer, X,Y Coordinate Block or blocks.
3. 5-Byte ASCII label (for netlist X reference)

Header Block
Address

0 Element Type

An ASCII character is used to select the element type.

'T'	track (no element label)
't'	track (with 5 Byte label for general reference)
'P'	pad (no element label)
'p'	pad (with 5 Byte label required for netlisting)
'B'	copper area (no element label)
'b'	copper area (with 5 Byte label for reference)
'W'	text (no element label)
'w'	text (with 5 Byte label for general reference)
$FF	end of file marker

Note EIX files set bit 7 of byte 4 to indicate 7 byte label.

---

1 Element Size

An ASCII character denotes element size i.e. '0','1','2' etc.
If element type is track or text the size represents width in mils * 5 i.e.: '1' = 5 mils.
If element type is copper area the size is not required and defaults to '0'.

If element type is pad then size represents 17 predefined shapes and sizes.

DEC	HEX	ASCII	Diameter	Shape
48	30	'0'	50	round
49	31	'1'	60	round
50	32	'2'	70	round
51	33	'3'	80	round
52	34	'4'	100	round
53	35	'5'	120	round
54	36	'6'	150	round
55	37	'7'	25	square
56	38	'8'	30	square
57	39	'9'	35	square
58	3A	':'	40	square
59	3B	';'	60	square
60	3C	'<'	80	square
61	3D	'='	200	bomb site
62	3E	'>'	200	round
63	3F	'?'	260	round
64	40	'@'		Thermal Power

---

2 Element Length

This equals the total number of 5-byte blocks in the Element Data Block. This value when multiplied by 5 will give the total number of bytes in this Element Data Block.

3+4 Library Reference

Note most significant byte is highest in memory.
Note EIX files set bit 7 of byte 4 to indicate 7 byte label of which the first 2 characters are stored here (bytes 3+4).

Coordinate Block
Address

0	Segment Layer This dictates the layer either for the Pad at coordinates held in this block or the track plotted from this Coordinate Block to the next. The system as it stands uses layers 0 to 16. Note that layer 16 has special properties in the editing environment but for netlisting it can be ignored.
1+2	X Coordinate in mils Note most significant byte is highest in memory.
3+4	Y Coordinate in mils Note most significant byte is highest in memory.

Further Coordinate Blocks may be present when:

1. If element is pad type then first block represents Pin 1 and second block represents Pin 2 and so on. If the element is a track type and the Library ID is within the range 8000 to 9999 then a finger pad is assumed. A finger pad's first and second Coordinate Blocks represent Pin 1 and the third and forth being Pin 2 and so on.
2. A track Via is created whenever a layer change occurs from one Coordinate Block to the next.
3. If element is copper area then only two Coordinate Blocks will exist i.e. coordinates of diagonally opposite corners.

Label Block (presence flagged by lower case of element type i.e. ‘P’ or 'p')
Address

0-4	Text Data 5 ASCII characters

APPENDIX C

Project File Format Version 2,3 (4.02 -)

From version 4.02 onwards a new project file format has been used to speed up processing and increase flexibility. The original format was designed for a Z80 based platform, hence the two's compliment integer form with the most significant byte highest in memory. The PCBDesign loader automatically detects format type and if need be converts the old formats to new. The data file consists of a File Information Element Block followed by a number of variable length Element Data Blocks terminated in a header block starting with hex FF.

Construction of the File Information Element
This is optional with Version 2, but required in all later versions.

File Information Blocks

Address		
0+1	Element Type $8000 = file information.	
2+3	Element Length Equals the total number of 6-byte blocks in the Element Data Block (including header and labels).This value when multiplied by 6 will give the total number of bytes in this Element Data Block.	
4	Project File Format Version number (2 -).	
5	Reserved	
6+7 8+9	X Cursor Coordinates in mils Y Cursor Coordinates in mils	
10+11	X Screen Offset in mils	
12+13	Y Screen Offset in mils	
14	Scale	
15	Grid Step	
16	Cursor Size	
17	Grid Overlay On & Colour	Bit 0 is active high on and bits 1-7 colour multiplied by 2
18+19	Reference ID Numbering Offset	
20	Display Mode 4,8,32,33	
30	New Layer Usage Flags	Bit 0=0 File has not had layers rearranged Bit 1=0 File was created with separate layers Bit 2=0 File was created assuming pads on layer 5 were also bottom resist
31	Active Colour Scheme 0,1,2	
32-47	Colour Mask Scheme 0	16 Layers Order of Layers: 10,0,1,4,2,17,8,9,3,5,6,7,15,16,13,14
48-63	Colour Mask Scheme 1	16 Layers Order of Layers: 10,0,1,4,2,17,8,9,3,5,6,7,15,16,13,14
64-79	Colour Mask Scheme 2	16 Layers Order of Layers: 10,0,1,4,2,17,8,9,3,5,6,7,15,16,13,14
80-209	NC Drill Sizes for Pads 0-129 (mm/10)	

File Information Blocks Extended Ver607

Address		
210-223	Creation Date	Format is 14 ASCII characters: 2009Sep2018:00
224+225	Block Width	
226+227	Block Height	
228	Label Track Width	0=5 mils 1=0mils, 2=5mils, 3=10mils, 4=15mils etc
229	High Density Track Mode	When Bit 0=1 all evenly numbered tracks, pads, and vias are reduced in size by 2 mils
230,231	Track Size, Layer	
232,233	Pad Size, Layer	
234	Block Layer	
235	Via Size	
236-239	Text Width, Height, Pen Size, Layer	

File Information Blocks Extended Ver658

Address	
240+241	Circle/ellipse Width
242+243	Circle/ellipse Height

File Information Blocks Extended Ver617

Address	
244-371	NC Drill Sizes for Pads 128-191 (mm/10)

File Information Blocks Extended Ver715

Address		
372-374	Layer On/Off	21 bits storing layer on/off status. 1=off, 0=on

File Information Blocks Extended Ver665

Address		
380-929	Layer Names	25 names. Each name is a fixed length record of 22 bytes. The first byte is the string length followed by the text string of 1-21 characters

File Information Blocks Extended Ver721

Address		
930-934	Colour Mask Scheme 0	4 Layers Order of Layers: 11,12,18,19
935-939	Colour Mask Scheme 1	4 Layers Order of Layers: 11,12,18,19
940-944	Colour Mask Scheme 2	4 Layers Order of Layers: 11,12,18,19

Construction of Element Data Block.

The construction of an Element Data Block consists of:

1. 6-Byte Header Block.
2. 6-Byte layer, size, X,Y Coordinate Block or blocks.
3. 18-Byte Label Blocks. These consist of a 12-Byte ASCII string followed by 6-Bytes of format information.

Header Block
Address

0+1	Element Type The most significant 4 bits select element type. Note bit 14 is always unset (this is used to detect file format Version 2 and above). $8000 = additional file information $0xxx = track $1xxx = text $2xxx = pad $3xxx = copper area $9xxx = polygon (not yet implemented) $Axxx = reserved $Bxxx = reserved $FFxx = end of file marker Label Blocks The least significant 12 bits hold the number of 6-byte blocks used for labels (3 blocks per label or 18 Bytes).
2+3	Element Length This equals the total number of 6-byte blocks in the Element Data Block (including header and labels). This value when multiplied by 6 will give the total number of bytes in this Element Data Block.
4+5	Library Reference The most significant 15 bits are used to store a library Reference ID (1 to 32000). Component Flag The most significant bit when set denotes component part. All elements that go to make up a component have this flag set apart from the first.

Coordinate Block
Address

0 Segment Layer

The least significant 6 bits dictate the segment layer either for the Pad at coordinates held in this block or the track plotted from this Coordinate Block to the next. Note that layer 63 has special properties in the editing environment but for netlisting it can be ignored.

Via Size

The most significant 2 bits are used to indicate via pad size.

Bits								Size
b7	b6	b5	b4	b3	b2	b1	b0	
0	0	X	X	X	X	X	X	50 mil
0	1	X	X	X	X	X	X	40 mil
1	0	X	X	X	X	X	X	30 mil
1	1	X	X	X	X	X	X	20 mil

---

1 Element Size

If element type is track or text then this selects width in mils * 5, for example '1' = 5 mils.

If element type is pad then the least significant 6 bits select the diameter in mils * 5 and the most significant 2 bits the shape and type.

Bits		Shape	
b7	b6		
0	0	round	
0	1	square	
1	0	thermal	(changed from specialised Version 6.17)
1	1	specialised	(Version 6.17 onwards)

The specialised pads selected by the least significant 6 bits are:

Bits								Shape	
b7	b6	b5	b4	b3	b2	b1	b0		
1	1	X	X	X	X	0	0	board marker	(changed from thermal Version 6.17)
1	1	X	X	X	X	0	1	reserved	(was board marker up to Version 6.16)
1	1	X	X	X	X	1	X	reserved	

2+3 X Coordinate in mils

4+5 Y Coordinate in mils

Further Coordinate Blocks may be present when:

1. If element is pad type then first block represents Pin 1 and second block represents Pin 2 and so on, but if two sequential pad coordinates are identical then these are assumed to be the same pin. If the element is a track type and the layers alternate between a visible and non visible layer (63) then a finger pad is assumed. A finger pad's non visible layers act as the pin count separators.
2. A track Via is created whenever a layer change occurs from one Coordinate Block to the next.
3. If element is copper area then Coordinate Blocks will only appear in pairs i.e. coordinates of diagonally opposite corners.

Label Block
Address

0-11	Text Data 12 ASCII characters. Note the Reference ID only has 10 characters.
10,11	Component Reference Offset A word offset added to the Reference ID used for panellizing several boards.
12	Text Layer The least significant 6 bits dictate the text layer. Bit 6 is reserved. Bit 7 is label display switch, 1-off 0-on
13	Text Attributes The least significant 6 bits dictate the Text Size (in 5 mil units). Bit 6 is label orientation 0 horizontal 1 vertical Bit 7 is label mirror 0 normal 1 mirrored
14+15	Text X Offset X offset from first Coordinate Block in mils.
16+17	Text Y Offset Y offset from first Coordinate Block in mils.

The first 6 label blocks have the following predefined usage.

1.	Reference ID	Example: ‘R1’
2.	Type/Value	Example: ‘220R’
3.	Modifier	Example: ‘0.063W’
4.	Footprint	Example: ‘0603’
5.	Supplier	Example: ‘Farnell’
6.	Supplier Stock Number	Example: ‘933-0801’

Any other label blocks are used for general labelling.

APPENDIX D

Project File Version Detection

1. If bit 6 of the first byte is set then the original version 1 format is assumed.
2. If the first byte is not $80 then the version 2 format is assumed.
3. If the first byte is $80 then the version number is found in the fifth byte.