GENERAL INSTRUMENT

27256

PRELIMINARY INFORMATION

256K (32K x 8) Bit NMOS UV Erasable PROM

FEATURES

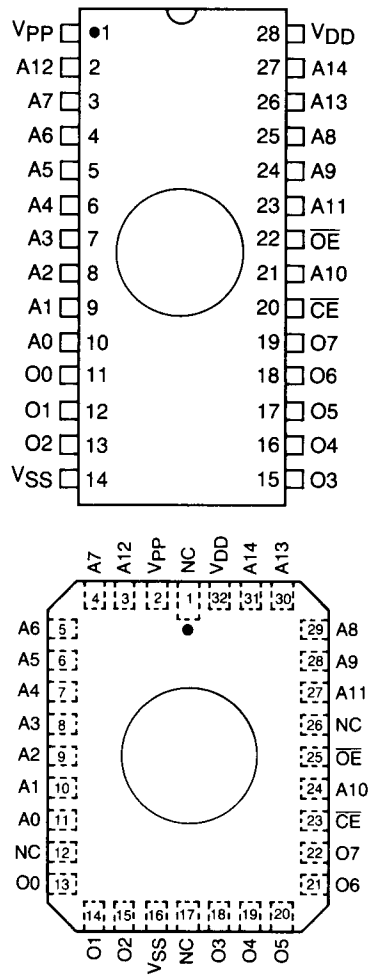
- High Speed Performance — 150ns Maximum Access Time
- Low Power Dissipation
  - — 100mA Active Current
  - — 40mA Standby Current
- Auto ID™ Identification; Aids Automated Programming
- Separate Chip Enable and Output Enable Control Inputs
- Two Programming Algorithms Allow Improved Programming Times
  - — Fast Programming
  - — Rapid-Pulse Programming
- Organized 32K x 8 — JEDEC Standard Pinouts
  - — 28-Pin Dual In Line Package
  - — 32-Pin Leadless Chip Carrier
- Available in Extended Temperature Ranges:
  - — Commercial (C) = 0° to 70°C
  - — Industrial (I) = −40° to +85°C
  - — Military (M)** = −55° to 125°C

DESCRIPTION

The General Instrument Microelectronics 27256 is a 256K bit ultraviolet light Erasable (electrically) Programmable Read Only Memory. The device is organized as 32K words by 8 bits (32K bytes). Accessing individual bytes from an address transition or from power-up (chip enable pin going low) is accomplished in less than 150ns. This very high speed device allows the most sophisticated microprocessors to run at full speed without the need for WAIT states.

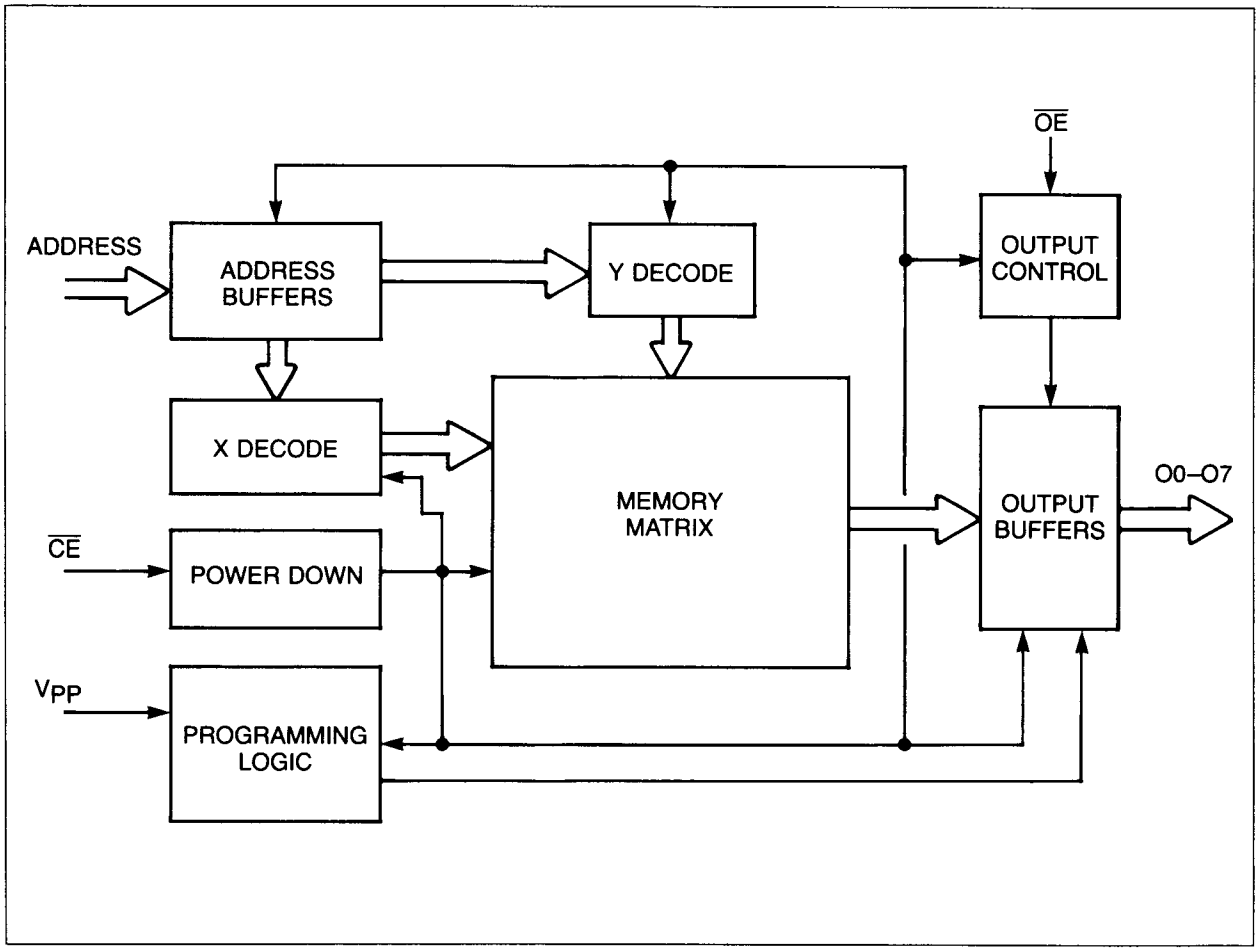
PIN CONFIGURATION

Top View



**Military Version (MR) screened to Mil. Std. 883 Rev. C, Method 5004 Test Specification.

BLOCK DIAGRAM



MODES

MODES	$\overline{CE}$	$\overline{OE}$	V_{PP}	A9	O0–O7
Read	V_{IL}	V_{IL}	V_{DD}	X	D_{OUT}
Program	V_{IL}	V_{IH}	V_H	X	D_{IN}
Program Verify	V_{IH}	V_{IL}	V_H	X	D_{OUT}
Program Inhibit	V_{IH}	V_{IH}	V_H	X	High Z
Standby	V_{IH}	X	V_{DD}	X	High Z
Output Disable	V_{IL}	V_{IH}	V_{DD}	X	High Z
Identity	V_{IL}	V_{IL}	V_{DD}	V_H	Identity Code

READ MODE (See Timing Diagrams and AC Characteristics)

Read mode is accessed when

a) the $\overline{CE}$ pin is low to power up (enable) the chip.
b) the $\overline{OE}$ pin is low to gate the data to the output pins.

For Read operations, if the addresses are stable, the address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is transferred to the output after a delay (t_{OE}) from the falling edge of $\overline{OE}$.

STANDBY MODE

The standby mode is defined when the $\overline{CE}$ pin is high and a program mode is not defined.

When these conditions are met, the supply current will drop from 100mA to 40mA.

OUTPUT ENABLE

This feature eliminates bus contention in multiple bus microprocessor systems and the outputs go to a high impedance when

- The $\overline{OE}$ pin is high and a program mode is not defined.

ERASE MODE

The memory matrix is erased to the all "1" 's state as a result of being exposed to ultraviolet light. To ensure complete erasure, a dose of 15 watt-second/cm^2 is required. This means that the device window must be placed within one inch and directly underneath an ultraviolet lamp with a wavelength of 2537 Angstroms and intensity of 12,000μ watt/cm^2 for 20 minutes.

PROGRAMMING MODE

Two programming algorithms are available. The fast programming algorithm is the industrial-standard programming mode that requires both initial programming pulses and overprogramming pulses. A flowchart of the fast programming algorithm is shown in Figure 1.

The rapid-pulse programming algorithm has been developed to improve on the programming throughput times in a production environment. Up to 25 100-microsecond pulses are applied until the byte is verified. No overprogramming is required. A flowchart of the rapid-pulse programming algorithm is shown in Figure 2.

Rapid-pulse is the preferred programming algorithm.

Programming takes place when

a) V_{PP} is brought to the proper V_H level
b) V_{DD} is brought to the proper level, and
c) the $\overline{OE}$ pin is high
d) the $\overline{CE}$ pin is low.

Since the erased state is "1" in the array, programming of "0" is required. The address to be programmed is set via A0–A14 and the data to be programmed is presented to O0–O7. When data and address are stable, a low-going pulse on the $\overline{CE}$ line programs that location.

VERIFY

After the array has been programmed it must be verified to ensure all the bits have been correctly programmed. This mode is entered when all the following conditions are met:

a) V_{PP} is at the proper V_H level
b) V_{DD} is at the proper level, and
c) the $\overline{CE}$ pin is high
d) the $\overline{OE}$ line is low.

INHIBIT

When programming multiple devices in parallel with different data, only $\overline{CE}$ need be under separate control to each device. By pulsing the $\overline{CE}$ line low on a particular device, that device will be programmed and all other devices with $\overline{CE}$ held high will not be programmed with the data (although address and data will be available on their input pins).

MANUFACTURERS IDENTITY

In this mode specific data is outputted that identifies the manufacturer as General Instrument Microelectronics, and the device type. This mode is entered when Pin (A9) is taken up to between 11.5V–12.5V. The $\overline{CE}$ and $\overline{OE}$ lines must be at V_{IL}. A0 is used to access any of the two non-erasable bytes whose data appears on O0 through O7.

The General Instrument Microelectronics identity code is as follows:

Pin / Identity	A0	D7	D6	D5	D4	D3	D2	D1	D0	Hex Code
Manufacturer	V_{IL}	0	0	1	0	1	0	0	1	29
Device Type*	V_{IH}	0	0	0	0	0	1	0	0	04

*Code subject to change.

ELECTRICAL CHARACTERISTICS
Maximum Ratings*

V_{DD} and input voltages w.r.t. V_{SS} ..... -0.6 to +6.25V
V_{PP} voltage w.r.t. V_{SS}
during programming ..... -0.6 to +14V
Voltage on A9 w.r.t. V_{SS} ..... -0.6 to +13.5V
Storage temperature ..... -65°C to +150°C
Ambient temperature with
power applied ..... -65°C to +125°C

Set Up Conditions for DC Characteristics (Read Operation)

V_{DD} = +5V ±10%
T_{AMB}: Commercial (C) = 0°C to 70°C
Industrial (I) = -40°C to +85°C
Military (M) = -55°C to +125°C

***Notice:** Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS (READ OPERATION)

PARAMETER	SYM	MIN	MAX	UNITS	CONDITIONS
Inputs					
Address lines A0-A14					
Data lines (program mode)					
O0–O7					
$\overline{CE}$ & $\overline{OE}$					
Logic "1"	V_{IH}	2.0	V_{DD}+1	V	
Logic "0"	V_{IL}	-0.1	0.8	V	
Leakage	I_{IL}	-10	10	μA	V_{IN} = 0 to V_{DD}
Input Capacitance	C_{IN}		6	pF	V_{IN} = 0V, T_{AMB} = 25°C, f = 1 MHz
Outputs					
In read/verify mode O0-O7					
Logic "1"	V_{OH}	2.4	—	V	I_{OH} = -400 μA
Logic "0"	V_{OL}		0.45	V	I_{OL} = 2.1 mA
Leakage	I_{OL}	-10	10	μA	V_{OUT} = 0 to V_{DD}
Output Capacitance	C_{OUT}		12	pF	V_{OUT} = 0V, T_{AMB} = 25°C, f = 1 MHz
Power Supply Current					
I_{DD} Active	I_{DD}		100	mA	V_{DD} = 5.5V, V_{PP} = V_{DD}, $\overline{OE}$ = $\overline{CE}$ = V_{IL}, T_{AMB} = −55°C to 125°C, I_{OUT} = 0 mA
I_{DD} Standby	I_{DD}(S)		40	mA	V_{DD} = 5.5V, T_{AMB} = 0 to 70°C, $\overline{CE}$ = V_{IH}, I_{OUT} = 0 mA
I_{DD} Standby (Extended Temp. Range)	I_{DD}(S)		45	mA	V_{DD} = 5.5V, T_{AMB} = −55°C to 125°C, $\overline{CE}$ = V_{IH}, I_{OUT} = 0 mA
I_{PP}(Read Mode)	I_{PP}		5	mA	V_{PP} = 5.5V (Note 2)
V_{PP} Read Voltage	V_{PP}	V_{DD}-0.7	V_{DD}	V	(Note 1)

NOTES: 1. V_{DD} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. V_{PP} may be connected directly to V_{DD} except during programming. The supply current would be the sum of I_{DD} + I_{PP}.

AC CHARACTERISTICS (Read Operation)

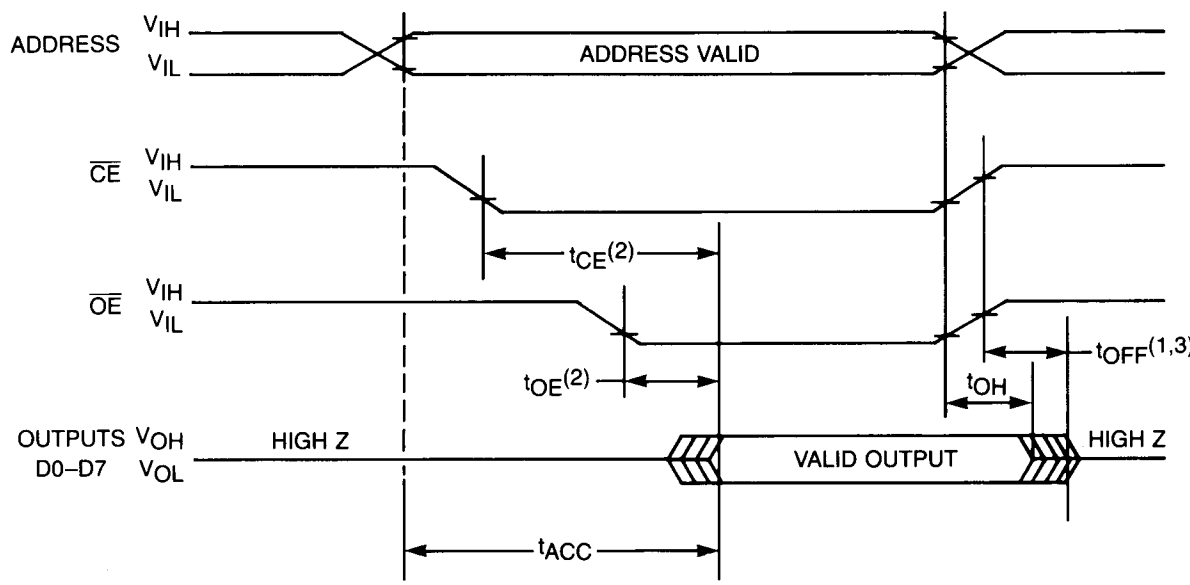
TA: Commercial (C) = 0°C to 70°C
Industrial (I) = -40°C to +85°C
Military (M) = -55°C to +125°C

AC TESTING WAVEFORM
V_{IH} = 2.4V AND V_{IL} = 0.45V
V_{OH} = 2.0V AND V_{OL} = 0.8V
Output Load = 1 TTL Load + 100 pF

Note: 27256-15 is only available in Commercial Temperature Range.

SYM	PARAMETER	27256-15		27256-17		27256-20		27256-25		UNITS	TEST CONDITIONS
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
t_{ACC}	Address To Output Delay		150		170		200		250	ns	$\overline{CE} = \overline{OE} = V_{IL}$
t_{CE}	$\overline{CE}$ To Output Delay		150		170		200		250	ns	$\overline{OE} = V_{IL}$
t_{OE}	$\overline{OE}$ To Output Delay		70		70		75		100	ns	$\overline{CE} = V_{IL}$
t_{OFF}	$\overline{OE}$ To O/P High Impedance	0	50	0	50	0	55	0	60	ns	$\overline{CE} = V_{IH}$
t_{OH}	Output Hold From Address $\overline{CE}$ or $\overline{OE}$, whichever occurred first	0		0		0		0		ns	

READ WAVEFORMS



NOTES:
(1) t_{OFF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.
(2) $\overline{OE}$ may be delayed up to t_{CE}-t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE}.
(3) This parameter is only sampled and not 100% tested.

DC PROGRAMMING CHARACTERISTICS

TA = 25 ± 5°C (See programming algorithm for V_{DD} and V_{PP} voltages.)

SYMBOL	PARAMETER	MIN	MAX	UNITS	CONDITIONS (SEE NOTE 1)
I_{LI}	Input Current (All Inputs)	-10	10	μA	$V_{IN} = V_{IL}$ or V_{IH}
V_{IL}	Input Low Level (All Inputs)	-0.1	0.8	V	
V_{IH}	Input High Level	2.0	$V_{DD}+1$	V	
V_{OL}	Output Low Voltage During Verify		0.45	V	$I_{OL} = 2.1$ mA
V_{OH}	Output High Voltage	2.4		V	$I_{OH} = -400$ μA
I_{DD2}	V_{DD} Supply Current (Program & Verify)		100	mA	
I_{PP2}	V_{PP} Supply Current (Program)		30	mA	$\overline{CE} = V_{IL}$
V_{ID}	A9 Produce Identification Voltage	11.5	12.5	V	

NOTES: 1. V_{DD} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.

AC PROGRAMMING CHARACTERISTICS

Conditions: 25°C ± 5°C.
(See programming algorithm for V_{DD} and V_{PP} voltages.)

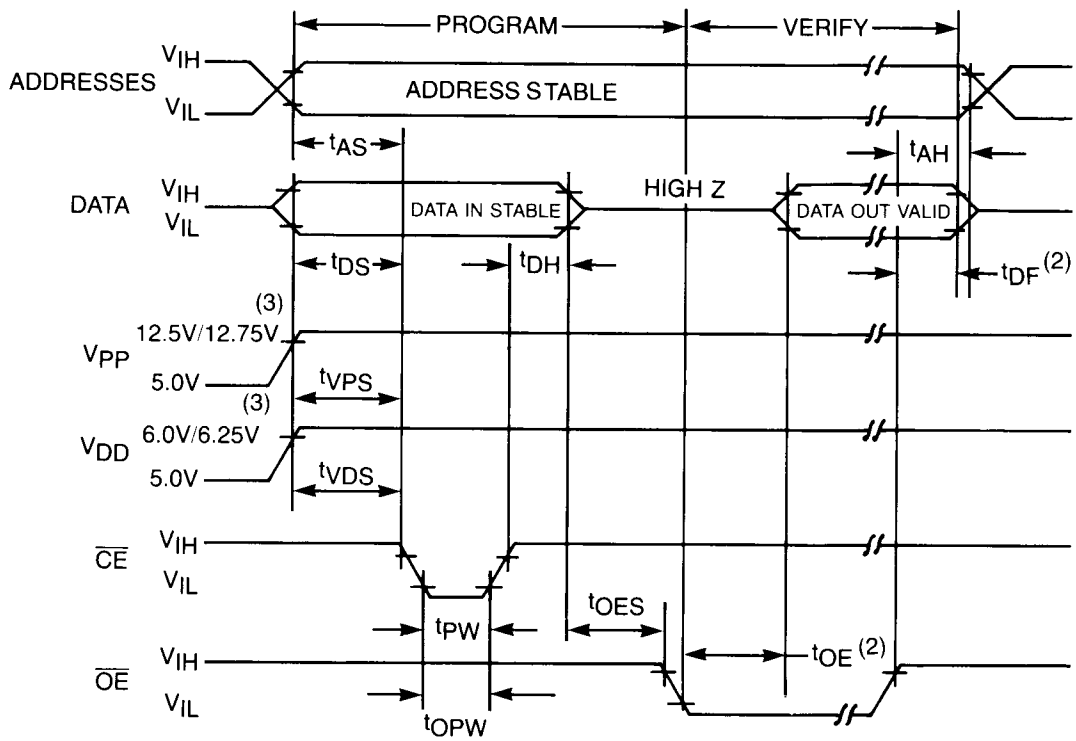
Program, Program Verify, and Program Inhibit Modes.

AC TESTING WAVEFORM
V_{IH} = 2.4V AND V_{IL} = 0.45V
V_{OH} = 2.0V AND V_{OL} = 0.8V
Output Load = 1 TTL Load + 100 pF

PARAMETER	SYM	MIN	TYP	MAX	UNITS
Address Set-Up Time	t_{AS}	2			μs
Data Set-Up Time	t_{DS}	2			μs
Data Hold Time	t_{DH}	2			μs
Address Hold Time	t_{AH}	0			μs
Float Delay[3]	t_{DF}	0		130	ns
V_{DD} Set-Up Time	t_{VDS}	2			μs
Program Pulse Width[1]	t_{PW}	0.95	1	1.05	ms
Program Pulse Width[1]	t_{PW}	95	100	105	μs
$\overline{CE}$ Set-Up Time	t_{CES}	2			μs
$\overline{OE}$ Set-Up Time	t_{OES}	2			μs
V_{PP} Set-Up Time	t_{VPS}	2			μs
Overprogram Pulse Width[2]	t_{OPW}	2.85		78.75	ms
Data Valid from $\overline{OE}$	t_{OE}			70	ns

NOTES:
1. For fast programming algorithm initial program pulse width tolerance is 1 ms ± 5%. For rapid-pulse programming algorithm initial programming pulse width tolerance is 100 μsec ± 5%.
2. For fast programming algorithm the length of the overprogram pulse may vary from 2.85 max to 78.75 ms as a function of the iteration counter value.
3. This parameter is only sampled and not 100% tested. Output float is defined as the point where data is no longer driven — See Timing Diagram.

PROGRAM WAVEFORMS[1]

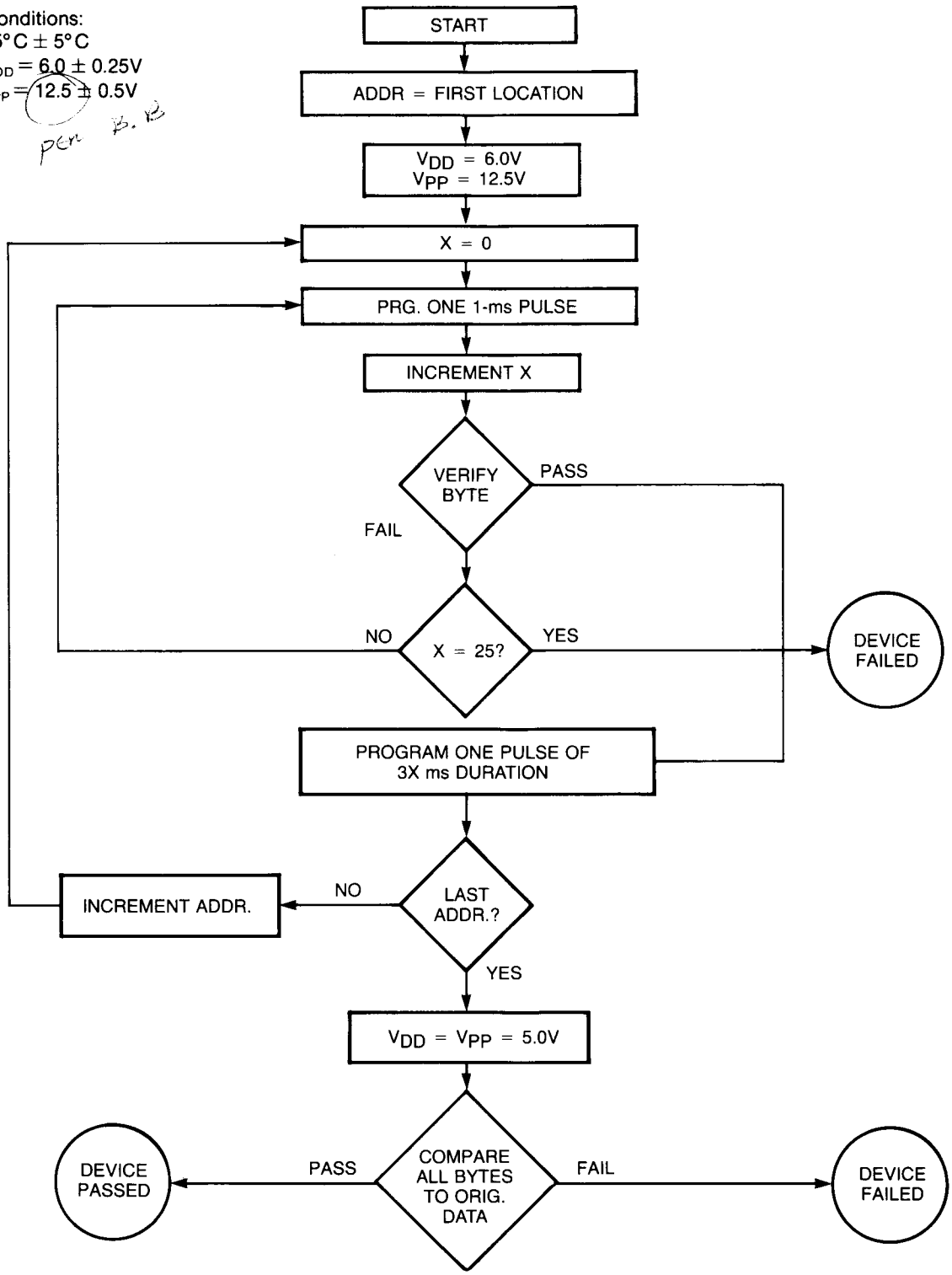


NOTES:

1. The input timing reference level is 0.8V for V_{IL} and 2.0V for V_{IH}.
2. t_{DF} on t_{OE} are characteristics of the device but must be accommodated by the programmer.
3. V_{DD} = 6.0 ± 0.25V, V_{PP} = 12.5 ± 0.5V for fast programming algorithm.
   V_{DD} = 6.25 ± 0.25V, V_{PP} = 12.75 ± 0.25V for rapid-pulse programming algorithm.

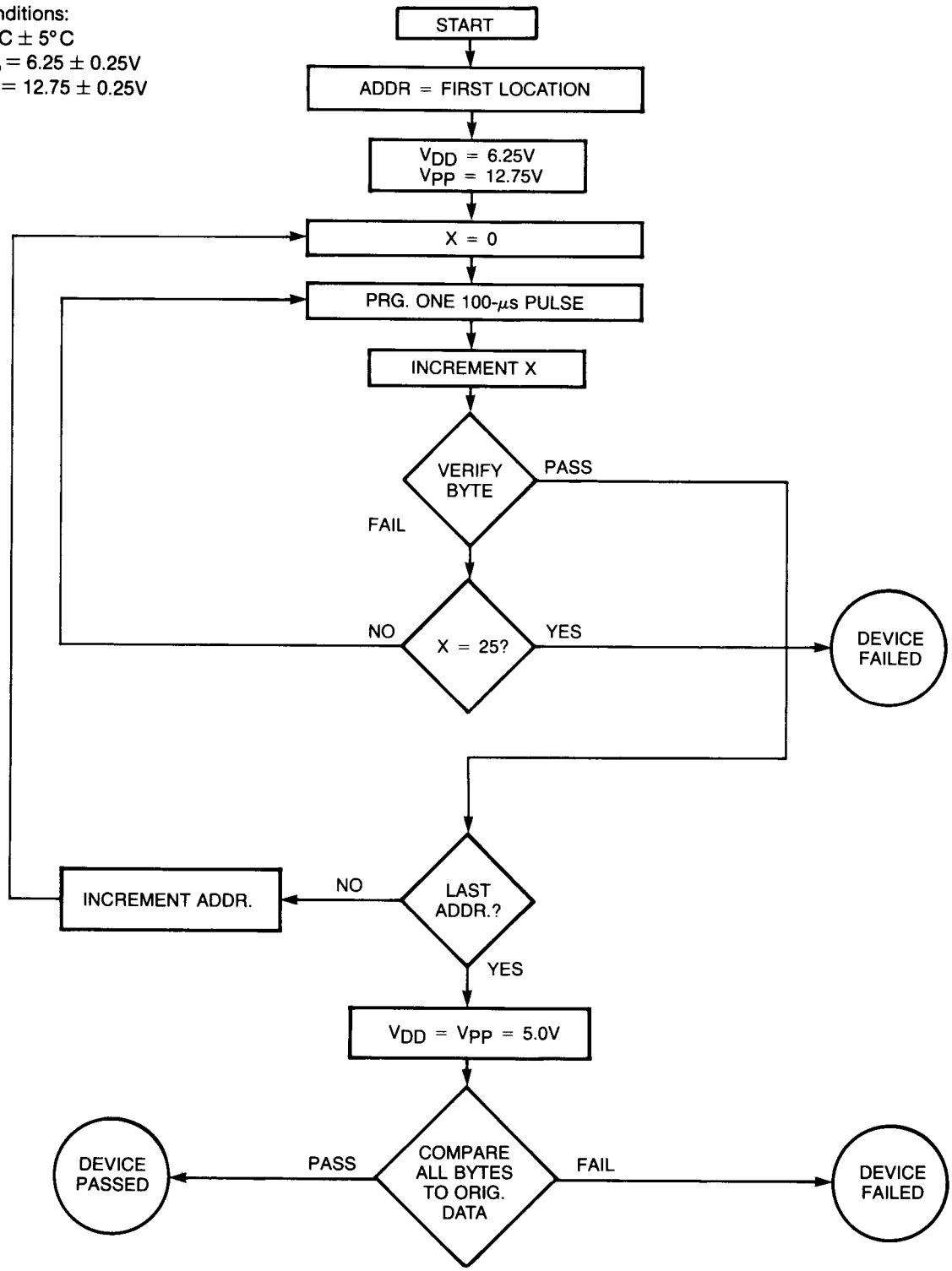
FAST PROGRAMMING ALGORITHM (Figure 1)

Conditions:
25°C ± 5°C
V_{DD} = 6.0 ± 0.25V
V_{PP} = 12.5 ± 0.5V



RAPID-PULSE PROGRAMMING ALGORITHM (Figure 2)

Conditions:
25°C ± 5°C
V_{DD} = 6.25 ± 0.25V
V_{PP} = 12.75 ± 0.25V



ORDERING INFORMATION

27256 -25 M R/ KA

PACKAGE
- — CERDIP
- D SIDEBRAZED CERAMIC
- KA CERAMIC LEADLESS CHIP CARRIER
- KB CERAMIC LEADLESS CHIP CARRIER, THERMALLY ENHANCE

SCREENING
- — STANDARD COMMERCIAL SCREENING
- R SCREENING PER MIL STD 883C METHOD 5004

TEMPERATURE RANGE
- — 0°C TO 70°C
- I -40°C TO 85°C
- M -55°C TO 125°C

SPEED
- -15 150 ns ACCESS
- -17 170 ns ACCESS
- -20 200 ns ACCESS
- -25 250 ns ACCESS

DEVICE
256K (32K X 8) EPROM

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