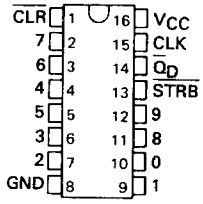
BULLETIN NO. DL-S 7211719, MAY 1972–REVISED DECEMBER 1972

FUNCTION TABLE

INPUTS			OUTPUTS	
COUNT PULSE (CLOCK)	CLEAR	LATCH STROBE	ON†	$\overline{Q}_D$
X	L	L	0	H
1	H	L	1	H
2	H	L	2	H
3	H	L	3	H
4	H	L	4	H
5	H	L	5	H
6	H	L	6	H
7	H	L	7	H
8	H	L	8	L
9	H	L	9	L
10	H	L	0	H
11	H	H	0	H

†All other outputs are off.
H = high level, L = low level, X = irrelevant

SN74142 . . . J OR N PACKAGE
(TOP VIEW)



description

The SN74142 contains a divide-by-ten (BCD) counter, a four-bit latch, and a decoder/*Nixie*‡ tube driver on a monolithic chip and is packaged in popular 16-pin packages. This single MSI function can replace the equivalent of three separately packaged MSI circuits to reduce printed-circuit board area and the number of system interconnections, resulting in reduced costs and improved reliability.

Four master-slave flip-flops are fully decoded to provide a divide-by-ten counter. A direct clear input will, when taken low, reset and hold the counter at zero (all Q outputs low, $\overline{Q}_D$ output high). While the clear input is inactive (high), each positive-going transition of the clock will increment the counter. The $\overline{Q}_D$ output is made available externally for cascading to n-bit counters.

The Q outputs of the counter are routed to the data inputs of the four-bit latch. While the latch strobe input is low, the internal latch outputs will follow the respective Q outputs of the counter. When the latch strobe input is taken high, the latch stores the data which has been setup by the counter outputs prior to the low-to-high level transition of the latch strobe input. The $\overline{Q}_D$ output from the counter is not stored by the latch since it is intended for clocking the next counter stage. This means that the system counter can continuously acquire new data. Since all outputs of the latch and Q outputs of the counter drive low-capacitance on-chip loads, the circuitry is considerably simplified with respect to the number of components required. This results in a highly efficient function which typically reduces power requirements 15% when compared to systems using the three separate packages.

The SN74142 counter/latch/driver features fully buffered inputs to reduce drive requirements to one normalized Series 74 load per input, and diode-clamping of all inputs to minimize transmission line effects. The counter will accept input clock frequencies up to 20 MHz and is entirely compatible for use with all popular TTL and DTL logic circuits. The high-performance n-p-n driver outputs are identical to the SN74141 and have a maximum off-state reverse current of 50 microamperes at 55 volts.

‡*Nixie* is a registered trademark of the Burroughs Corporation.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Off-state current into outputs 0 thru 9 . . . . . 1 mA
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: All voltage values are with respect to the network ground terminal.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
High-level output current from $\overline{Q}_D$, I_{OH}				−400	μA
Low-level output current from $\overline{Q}_D$, I_{OL}				8	mA
Input clock frequency, f_{clock}		0		20	MHz
Clock pulse width, $t_{w(clock)}$ (see Figure 1)	High logic level	15			ns
	Low logic level	35			
Clear pulse width, $t_{w(clear)}$ (see Figure 1)		25			ns
Strobe pulse width, $t_{w(strobe)}$ (see Figure 1)		20			ns
Clear inactive-state setup time, t_{su} (see Figure 1)		25			ns
Strobe time, t_{strobe} (see Figure 1)		45		$t_{w(clock)}$ +10	ns
Operating free-air temperature, T_A		0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −12 mA			−1.5	V
V_{OH}	High-level $\overline{Q}_D$ output voltage	V_{CC} = MIN, I_{OH} = −400 μA	2.4	3.4		V
V_{OL}	Low-level $\overline{Q}_D$ output voltage	V_{CC} = MIN, I_{OL} = 8 mA		0.2	0.4	V
$V_{O(on)}$	On-state voltage, outputs 0 thru 9	V_{CC} = MIN, I_O = 7 mA			2.5	V
$V_{O(off)}$	Off-state voltage, outputs 0 thru 9	V_{CC} = MAX, I_O = 0.5 mA	60			V
$I_{O(off)}$	Off-state current, outputs 0 thru 9	V_{CC} = MAX, V_O = 55 V			50	μA
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V			1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V			−1.6	mA
I_{OS}	Short-circuit $\overline{Q}_D$ output current	V_{CC} = MAX	−18		−55	mA
I_{CC}	Supply current	V_{CC} = MAX, All outputs open		68	102	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level $\overline{Q}_D$ output from clock	C_L = 15 pF, R_L = 800 Ω, See Figure 1		35	55	ns
t_{PHL}	Propagation delay time, high-to-low-level $\overline{Q}_D$ output from clock			30	45	
t_{PLH}	Propagation delay time, low-to-high-level $\overline{Q}_D$ output from clear			30	45	ns

TEXAS INSTRUMENTS
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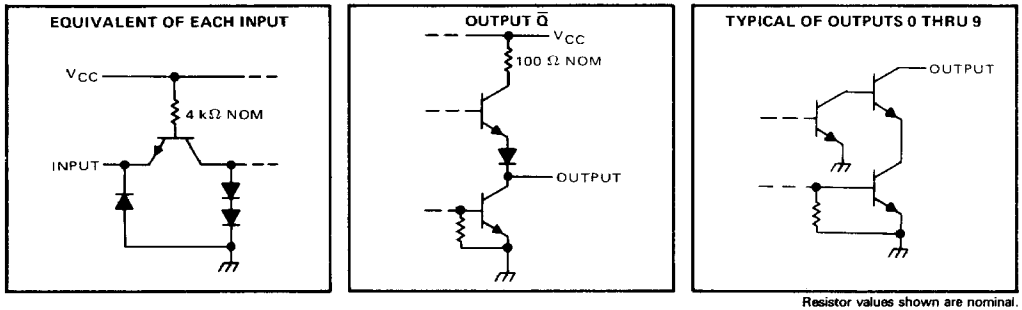
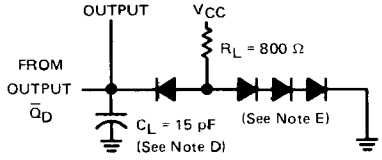
schematics of inputs and outputs

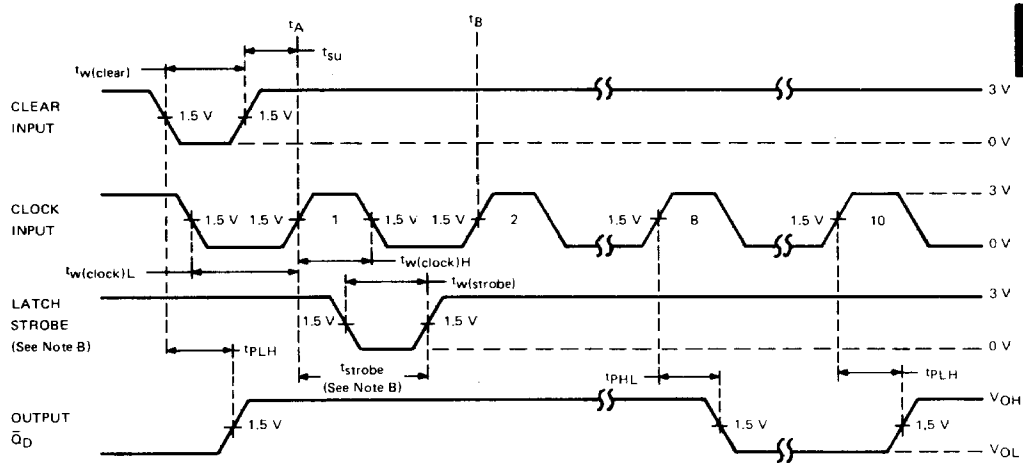


Resistor values shown are nominal.

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. This typical abbreviated sequence illustrates clearing from count 8 or 9 and counting through ten clock pulses. Clock pulses 3 through 7 and 9 are omitted for brevity.

B. Strobe input can go low at any time; however, the positive transition to store data from any given clock transition (t_A) must occur a minimum of 45 ns after t_A and prior to 10 ns after the next positive-going clock transition (t_B + 10 ns).

C. Input pulses are supplied by generators having the following characteristics: $t_r \leq 7$ ns, $t_f \leq 7$ ns, PRR = 1 MHz, and $Z_{out} \approx 50\ \Omega$.

D. C_L includes probe and jig capacitance.

E. All diodes are 1N3064 or equivalent.

FIGURE 1