MK 14
VDU Instructions

The MK14 VDU is memory mapped and works by DMA (Direct Memory Access) of the MK14 memory. It must be connected to the address bus and the data bus of the MK14. Each time the VDU needs to read the memory (so that it can display its contents), the VDU sends a signal to stop the SCMP (this signal is called NENIN). It then takes NRDS low and counts up twice through the addresses on A0 – A7 meanwhile displaying their contents. The memory page (1 page = 256 bytes) selected depends on the inputs PS1 – PS4 (page selects) which correspond to A8 → A11. If these are changed half way through a vertical scan of the TV two different pages may be displayed. The VDU requires only a +5 volts stabilised power supply from the MK14 regulator. A heatsink will be necessary.

Construction Notes.

1. We recommend you use sockets for all the integrated circuits.
2. When soldering use a minimum of solder and a fine tipped soldering iron.
3. The holes are plated through and you should not solder both sides of the board.
4. Check the board carefully for any flaws.
5. Carefully read all the notes we supply. If you are truly uncertain about how to proceed contact us for more information.
6. Use reasonable caution when handling CMOS components.

Component List.

Part Number	Value	Remarks
R1, R16	470	Yellow Violet Brown
R2, R11, R14, R17	1K2	Brown Red Red
R3, R4	27K	Red Violet Orange
R5, R7, R10, R12, R13, R15	4K7	Yellow Violet Red
R8	2K4	Red Yellow Red
R9	150	Brown Green Brown
R6	–	Not required
C1, C2, C3, C4, C5, C6, C7		Any value between 30N and 100N
C8	~~6N8~~ 10n	~~6N8 or 682~~ 0.01
C9	220	220K or 221
C10	–	Not required
C11	~~.82~~ 100	~~82J~~ 101
D1		Blue body. White band + ve.
Q1, Q2, Q3, Q4	BC239	
IC1	74L86	
IC2	74LS20	May be 74L20
IC3	74LS93	
IC4	74LS74	May be 74L74
IC5	4011	May be 5611
IC6	4040	May be 5640
IC7, IC12	74LS04	May be 74L04
IC8	74LS157	May be 81L22 or 74L157
IC9, IC10	80L95	
IC11	74LS27	
IC13	4012	May be 5612
IC14	74LS00	May be 74L00
IC15	DM8678CAB	Character generator
IC16	74LS165	May be 8590

Astec UM1233 Modulator
Printed Circuit Board.

First of all make the following connections. If you have an issue 4 or issue 5 board the connections can be made through a double sided connector at the top of the MK14 board.

VDU connection*	Name	MK14 connection	Remarks
a1	0V	pin 20 of IC1	Zero volts
a2	A0	pin 25 "	Address bus
a3	A1	pin 26 "	"
a4	A2	pin 27 "	"
a5	A3	pin 28 "	"
a6	A4	pin 29 "	"
a7	A5	pin 30 "	"
a8	A6	pin 31 "	"
a9	A7	pin 32 "	"
a10	A8	pin 33 "	"
a11	A9	pin 34 "	"
a12	A10	pin 35 "	"
a13	A11	pin 36 "	"
a18	D0	pin 16 "	Data bus
a19	D1	pin 15 "	"
a20	D2	pin 14 "	"
a21	D3	pin 13 "	"
a22	D4	pin 12 "	"
a23	D5	pin 11 "	"
a24	D6	pin 10 "	"
a25	D7	pin 9 "	"
a28	NRDS	pin 2 "	Negative read strobe
a31	NENIN	pin 3 "	Stop processor
a32	+5V	pin 40 "	Power supply

*looking at the component side of the PCB, row a is closest to the end of the board and connections 32 are at the side nearest to Q3 and Q4.

VDU connection	Name	MK14 connection	Remarks
b9	PS1		
b10	PS2	Hard wired to +5V,	These determine which pages are displayed by the
b11	PS3	0V, or an IO port	VDU. As a first test connect PS1, PS2, PS3, PS4
b12	PS4		to 0V.
b13	VDU OFF	FLAG 1	Take low (natural state on reset) to turn VDU on.
b14	GRAPHICS/CHARS	Can connect to flag or be switched	Take low for character mode, high for graphics.
b15	REVERSE PAGES	"	Take low to reverse top and bottom pages.
b16	INVERT VIDEO	"	Take low to give reverse video (black on white).
b17	TOP PAGE	—	High when first half of TV picture displayed.
b27	XOUT	pin 38 of IC1	Clock signed at 4Mhz. (not 4.43 Mhz).

It is also necessary to make the following modifications to the MK14 board.

1. Connect a 4K7 resistor from NWDS (pin 1 of IC1) to +5V (pin 40 of IC1).
2. Cut the connection from pin 3 of IC1 (NENIN) to 0V.
3. Cut the connection from pin 3 of IC1 to pin 15 of IC10.
4. Remake connection from pin 15 of IC10 to 0V.

When first testing the VDU connect b9 – b12 to 0V and leave b14 – b17 unconnected. On powering up the MK14 the LED display should work normally. If the output of the UHF modulator is connected to the aerial socket of a UHF TV you should be able to find a strong signal from the VDU on channel 36 showing a bit-map of the monitor.

You will notice that the top half and lower half of the screen are the same. Now disconnect b11 from 0V and connect it to b17. The screen will now display the first two ¼K pages of memory (the monitor PROM). If you connect b16 to 0V the picture will invert. If you connect b14 to 0V the display will show the contents of memory as ASCII characters. If you connect b15 to ground the top and bottom pages will swap round.

Next try connecting b9, b11 and b12 through a 1K resistor to +5V. The VDU will now display the normal RAM (0F00 – 0FFF) and extra RAM (0B00 → 0BFF) on the screen. Notice how some locations flicker as they are continuously changed by the program in the monitor PROM. This flicker disappears if the RESET button is depressed. Try connecting b14 to b17 to produce a display which is part graphics and part characters. Notice that you can change the characters by writing new values into the extra RAM area (20_{16} corresponds to a space). You can change the pattern in the graphics area by writing into 0F12 → 0FFF. (00_{16} corresponds to a blank). Notice how the eight bits of each byte are spread out in a row.

Finally write 02 into 0FFF and press GO. (This is a quick way of setting FLAG 1). The VDU display should blank and the MK14 will run at full speed so that you can load taped programs. Press reset to turn on the VDU again.

NB: When running the VDU causes program execution to run about 6% slower.

The following three programs illustrate how to use an MK14 fitted with the extra RAM, RAM–I/0 chip and VDU. If the Extra RAM and normal RAM are displayed by the VDU the only RAM area remaining for user program is the RAM of the RAM-I/0 chip. The following three programs fit into these 80_{16} bytes. One can of course use part of the VDU RAM for larger user programs but then they will appear on the display. It is straightforward to add more RAM if this proves necessary.

BIT is a subroutine that can be used to turn on and off and read the spots of a graphics display. It forms the basis of a graphics program. (b14 should be taken to +5V through a 1K resistor).

PUTC is a subroutine which makes the MK14 VDU behave like a standard VDU. It puts the ASCII character corresponding to the byte in the accumulator (lower six bits only) onto the screen in consecutive locations and handles the codes for Carriage Return, Line Feed, Vertical Tab, Backspace and Horizontal Tab. (b14 should be wired to 0V).

SHOWCH is a short demonstration program which clears the screen and then displays the font of the character generator. (b14 should be wired to 0V).

A Short Technical Description.

The MK14 VDU uses a 74LS74, a 74LS93 and a 4040 as a counter chain to count the 312 lines of a TV display and to generate row and column addresses for character or graphics display.

A 74LS157 is used to select the different mappings required for graphics bit map (eight bytes in a row) and for character display (16 bytes in a row). Two 80L95s isolate the VDU from the address and data bus when it is being used by the SCMP. A 4011 generates the sync pulse waveforms. A 74L86 is used to invert the video and buffer the CMOS. Further buffering is performed by the two 74LS04s.

A 74LS165 parallel in/serial out shift register generates the graphics by shifting out the data read on the databus and a DM8678 character generator chip is used to generate ASCII characters from the lower six bits of the databus.

The other chips control the use of the address and databus by the SCMP and VDU and provide the necessary signals for the shift register and character generator.

Two transistors are used to buffer NENIN, XOUT and a further two to form a composite video signal which is fed into the onboard modulator.

BIT PROGRAM FOR MK14 VDU

```
0880  02          BIT   CCL          P1 should point to the page to be displayed.
0881  CAFF              ST BIT(2)    This routine requires P2 to point to a stack.
0883  C201              LD Y(2)      0(2) should contain X and 1(2) contain Y
0885  IE                RR           where 0<X<63 and 0<Y<31.  Values outside
0886  IE                RR           these ranges are mapped on modulo 64 and 32.
0887  IE                RR           If on entry the accumulator contains
0888  IE                RR           a) 00 the bit at (X,Y) is cleared.
0889  IE                RR           b) 01 the bit at (X,Y) is set
088A  D4F8              ANI X'F8     c) FF the bit at (X,Y) is read and the value
088C  01                XAE          returned in the accumulator (0 for zero).
088D  C200              LD X(2)
088F  1C                SR
0890  1C                SR
0891  1C                SR
0892  D407              ANI X'07
0894  70                ADE
0895  31                XPAL 1       X and Y are used to calculate PIL.
0896  C200              LD X (2)
0898  D407              ANI X'07
089A  02                CCL
089B  F424              ADI X'24     Use PC relative extension register addressing
089D  01                XAE          to obtain a suitable mask for the bit
089E  C080              LD E(0)      corresponding to (X, Y).
08A0  CAFE              ST MASK (2)
08A2  C2FF              LD BIT (2)
08A4  940A              JP PUT
08A6  C100        GET:  LD 0(1)      Read bit
08A8  D2FE              AND MASK (2)
08AA  9814              JZ RET
08AC  C401              LDI X'01
08AE  9010              JMP RET
08Bo  9802        PUT:  JZ S         If zero clear a bit.
08B2  C2FE              LD MASK (2)  Set a bit
08B4  01          S:    XAE
08B5  C2FE              LD MASK (2)
08B7  E4FF              XRI X'FF
08B9  D500              AND 0(1)
08BB  70                ADE
08BC  C900              ST 0(1)
08BE  C2FF              LD BIT (2)
08C0  3F          RET:  XPPC 3
08C1  90BD              JMP BIT
08C3  8040201008040201             Table of mask values
```

SHOW CHARS ON MK14 VDU

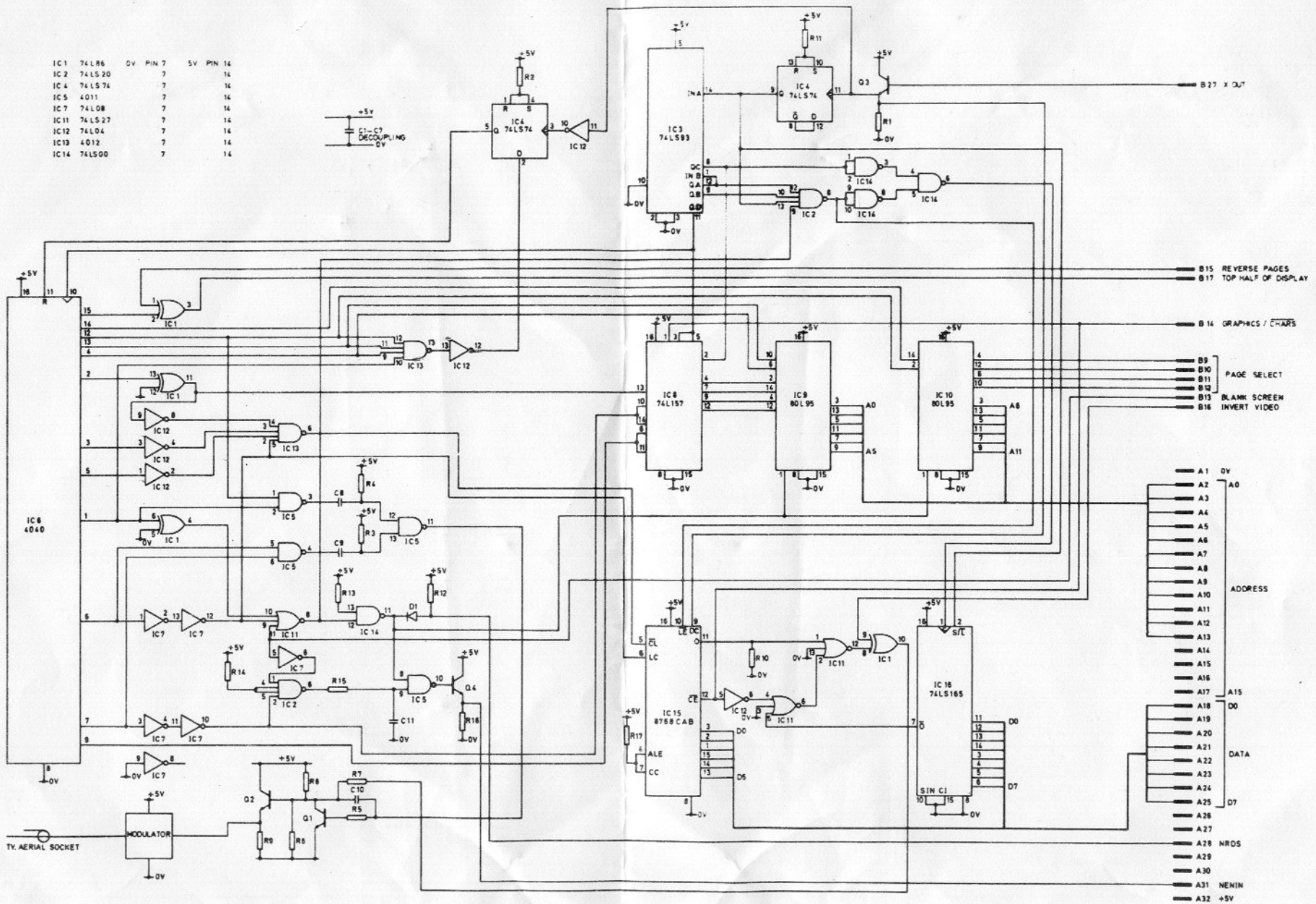
```
0880  C40F  SHOWCH  LDI X'0F
0882  35            XPAH 1
0883  C400  S1      LDI X'00
0885  31      S2    XPAL 1
0886  C420          LDI X'20
0888  CD01          ST @ 1(1)
088A  31            XPAL 1
088B  9CF8          JNZ S2
088D  35            XPAH 1
088E  E40C          XRI X'0C
0890  9804          JZ S3
0892  C40B          LDI X'0B
0894  90EC          JMP S1
0896  31      S3    XPAL 1
0897  C40B          LDI X'0B
0899  35            XPAH 1
089A  C443          LDI X'43
089C  C902          ST 2(1)
089E  C448          LDI  X'48
08P0  C903          ST 3(1)
08A2  C441          LDI X'41
08A4  C904          ST 4(1)
08A6  C452          LDI X'52
08A8  C905          ST 5(1)
08AA  C43D          LDI X'3D
08AC  C906          ST 6(1)
08AE  A807  S4      ILD 7(0)
08B0  C907          ST 7 (1)
08B2  8FFF          DLY X'FF
08B4  90F8          JMP S4
```

This routine requires only the RAM-I/O chip and Extra RAM to be fitted. It first blanks the screen and then displays the character set.

PUTC ROUTINE FOR MK14

```
0880  01    PUTC  XAE
0881  02          CCL
0882  C40B        LDI H(EXTRA RAM)
0884  35          XPAH 1
0885  40          LDE
0886  E40D        XRI 00D
0888  981B        JZ CR
088A  E407        XRI 007
088C  981C        JZ LF
088E  E401        XRI 001
0890  981D        JZ VT
0892  E403        XRI 003
0894  9828        JZ BS
0896  E401        XRI 001
0898  9803        JZ HT
089A  40          LDE
089B  C900        ST 0(1)
089D  31    HT    XPAL 1
089E  F401        ADI 001
08A0  31    S2    XPAL 1
08A1  40          LDE
08A2  3F          XPPC 3
08A3  90DB        JMP PUTC
08A5  31    CR    XPAL 1
08A6  D4F0        ANI 0F0
08A8  90F6        JMP S2
08AA  31    LF    XPAL 1
08AB  F410        ADI 010
08AD  90F1        JMP S2
08AF  C400  VT    LDI 000
08B1  CAFF        ST-1(2)
08B3  31    S1    XPAL 1
08B4  C420        LDI 020
08B6  C900        ST 0(1)
08B8  AAFF        ILD-1(2)
08BA  9CF7        JNZ S1
08BC  90E2        JMP S2
08BE  31    BS    XPAL 1
08BF  F4FF        ADI 0FF
08C1  90DD        JMP S2
```

The character whose ASCII code is in the accumulator is written to the next character cell on the screen. Carriage Return, Line Feed, Vertical Tab, Backspace and Horizontal Tab are interpreted.


IC 1 74L86 0V PIN 7 5V PIN 14
IC 2 74LS 20 7 14
IC 4 74LS 74 7 14
IC 5 4011 7 14
IC 7 74L08 7 14
IC 11 74LS 27 7 14
IC 12 74L04 7 14
IC 13 4012 7 14
IC 14 74LS00 7 14
C1-C7 DECOUPLING 0V
+5V
0V
R1
R2
R3
R4
R5
R6
R7
R8
R9
R10
R11
R12
R13
R14
R15
R16
R17
C8
C9
C10
C11
D1
Q1
Q2
Q3
Q4
IC 1
IC 2
IC 4 74LS74
IC 5
IC 7
IC 11
IC 12
IC 13
IC 14
IC 3 74LS93
IC 6 4040
IC 8 74L157
IC 9 80L95
IC 10 80L95
IC 15 8788 CAB
IC 16 74LS165
MODULATOR
TV. AERIAL SOCKET
B27 X OUT
B15 REVERSE PAGES
B17 TOP HALF OF DISPLAY
B14 GRAPHICS / CHARS
B9
B10
B11
B12
PAGE SELECT
B13 BLANK SCREEN
B16 INVERT VIDEO
A0
A5
A6
A11
A1 0V
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
A12
A13
A14
A15
A16
A17 A15
A18 D0
A19
A20
A21
A22
A23
A24
A25 D7
ADDRESS
DATA
A26
A27
A28 NRDS
A29
A30
A31 NENIN
A32 +5V